AMPAK Technology Inc.

正基科技股份有限公司

SPECIFICATION

PRODUCT NAME：AP12612X_M2

REVISION：0.1

DATE：Apr. 2nd , 2025

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		

正基科技股份有限公司

AMPAK Technology Inc.

AP12612X_M2

Data Sheet

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Revision

Revision	Date	Description	Revised By
01	2025/04/02	- Preliminary	May

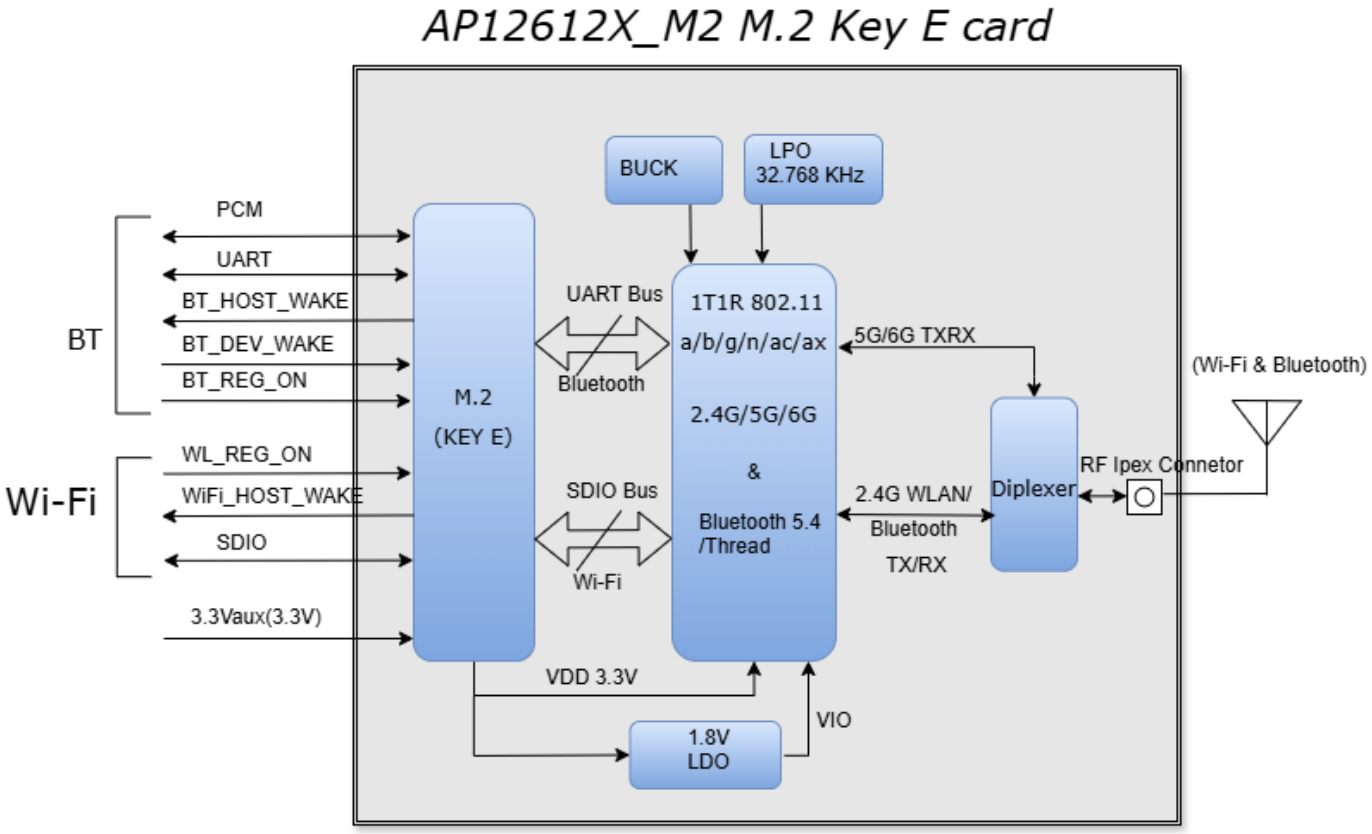
Contents

1. Introduction

1.1 Overview

The AMPAK Technology® AP12612X_M2 is a fully Wi-Fi 6E and Bluetooth functionalities module with seamless roaming capabilities and advance security. It is capable of associating with variety of Wi-Fi 6E or legacy Access Points / Routers Furthermore, AP12612X_M2 supports SDIO v3.0 / 2.0 interfaces by proper setting for Wi-Fi and UART/ PCM interface for Bluetooth.

In addition, this compact module is a total solution for a combination of Wi-Fi + Bluetooth technologies. The module is specifically developed for tablet, OTT box and portable & mobile devices.



1.2 Product Features

IEEE 802.11 Key Features

- 11ax,1x1 20MHz Tri band support WiFi6E 2.4G, 5G and 6GHz
- SDIO with 50 Mbps max throughput (supports up to MCS9 with AMPDU capped at 4 MPDUs)
- SoftAP/P2P (with up to 2 connections)
- Extensive offload schemes (Packet filtering, Roaming, ARP, Keep Alive etc.)
- 802.11h, 802.11r, 802.11i, 802.11v, 802.11w
- WiFi6E, WMM, PMF certified
- Secure Boot and WPA3 R3 supported
- Coexistence scheme: Shared LNA.

Bluetooth Key Feature

- BT 5.4 or BT 6 (Channel Sounding) dual mode controller
- BDR (1Mbps) / EDR (2Mbps, 3Mbps) / LE (1Mbps, 2Mbps, 500kbps, 125kbps)
- LE Audio Unicast and Aura cast Support
- High Rate (8Mbps, 4Mbps, 2Mbps)
- A2DP offloading (raw PCM, I2S packetized)
- LE audio offloading (I2S packetized) with bi-directional support
- eSCO (CVSD, mSBC, LC3)
- Thread and 802.15.4 support

2. General Specification

2.1 General Specification

Model Name	AP12612X_M2
Product Description	1T1R 802.11 a/b/g/n/ac/ax Wi-Fi 6E + BLUETOOTH 5.4 + 802.15.4 2230 M.2 card (KEY E)
Dimension	L x W : 30 x 22 mm (typical); H :2.7 mm (max.)
Wi-Fi Interface	Support SDIO V3.0/2.0
BLUETOOTH Interface	UART / PCM
Operating temperature	-40°C to +85°C
Storage temperature	-40°C to +125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.2V < VBAT < 3.6V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
3.3Vaux	Input supply voltage	-0.5	4.5	V
WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section.	-0.5	3.9	V
BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section.			
Digital Bus	UART / PCM Bus			
WL_HOST_WAKE	WLAN device wake-up HOST			
BT_HOST_WAKE	Bluetooth device wake-up HOST			
BT_DEV_WAKE	HOST wake-up Bluetooth device			

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	Condition	ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

2.2.2 Recommended Operating Rating

Voltage rails	Min.	Typ.	Max.	Unit
3.3Vaux	3.0	3.3	3.6	V
WL_REG_ON	1.62	1.8	1.98	V
BT_REG_ON				
Digital Bus				
WL_HOST_WAKE				
BT_HOST_WAKE				
BT_DEV_WAKE				

3.3Vaux current consumption 1200mA(Peak), when 3.3Vaux = 3.3V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
Input high voltage	0.65 x VDDIO	NA	V
Input low voltage	NA	0.35 x VDDIO	V
Output high voltage @ 2mA	VDDIO – 0.4	NA	V
Output low voltage @ 2mA	NA	0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp=25°C

Feature	Description
WLAN Standard	IEEE 802.11 b/g/n/ax & Wi-Fi compliant
Frequency Range	2400 MHz ~ 2483.5 MHz (2.4GHz ISM Band)
Number of Channels	2400 MHz ~ 2483.5 MHz：Ch1 ~ Ch13
Modulation	802.11b : DQPSK、DBPSK、CCK 802.11g/n : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ax : OFDMA /256-QAM、64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 1.5 dB

The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	19	19	19	19	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	19	19	18	18	17
	54Mbps				
	17				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	18.5	18.5	18	17	16
	MCS7				
	16				
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6
	18.5	18.5	18	17	16
	HE7	HE8	HE9		
	16	15.5	15		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB

CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%

802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-98		
	2Mbps	-94		
	5.5Mbps	-92		
	11Mbps	-88.5		

802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92.5	24Mbps	-84
	9Mbps	-90	36Mbps	-81
	12Mbps	-88	48Mbps	-78
	18Mbps	-86	54Mbps	-76
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS4	-79
	MCS1	-89	MCS5	-77
	MCS2	-86	MCS6	-76
	MCS3	-82	MCS7	-74
802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-92	HE6	-76
	HE1	-89	HE7	-74
	HE2	-86	HE8	-72
	HE3	-82	HE9	-70.5
	HE4	-79		
	HE5	-77		
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n/ax : -20 dBm			

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp=25°C

Feature	Description
WLAN Standard	IEEE 802.11a/n/ac/ax & Wi-Fi compliant
Frequency Range	5150~5350MHz、5470~5725MHz、5725~5850MHz (5GHz UNII Band)
Number of Channels	5150~5350MHz：Ch36 ~ Ch64 5470~5725MHz：Ch100 ~ Ch140 5725~5850MHz：Ch149 ~ Ch165
Modulation	802.11a : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11n : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ac : OFDM /256-QAM、64-QAM、16-QAM、QPSK、BPSK 802.11ax : OFDMA /1024-QAM、256-QAM、64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 2 dB

The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11a	**Frequency (MHz)**	**6~9Mbps**	**12~18Mbps**	**24Mbps**	**36Mbps**
	5150~5350	15.5	15.5	15.5	15.5
	5470~5725	15.5	15.5	15.5	15.5
	5725~5850	15.5	15.5	15.5	15.5
	Frequency (MHz)	**48Mbps**	**54Mbps**		
	5150~5350	15.5	15		
	5470~5725	15.5	15		
	5725~5850	15.5	15		
802.11n 20MHz	**Frequency (MHz)**	**MCS0~2**	**MCS3**	**MCS4**	**MCS5**
	5150~5350	15.5	15.5	15.5	15.5
	5470~5725	15.5	15.5	15.5	15.5
	5725~5850	15.5	1.5	15.5	15.5
	Frequency (MHz)	**MCS6**	**MCS7**		
	5150~5350	15	14		
	5470~5725	15	14		
	5725~5850	15	14		

802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5725	15.5	15.5	15.5	15.5
	5725~5850	15.5	1.5	15.5	15.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	15	14	12.5	
	5470~5725	15	14	12.5	
	5725~5850	15	14	12.5	
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15.5	15.5	15.5	15.5
	5470~5725	15.5	15.5	15.5	15.5
	5725~5850	15.5	1.5	15.5	15.5
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15	14	12.5	11.5
	5470~5725	15	14	12.5	11.5
	5725~5850	15	14	12.5	11.5
	Frequency (MHz)	HE10	HE11		
	5150~5350	9.5	9.5		
	5470~5725	9.5	9.5		
	5725~5850	9.5	9.5		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB

CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%

802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-83
	9Mbps	-89	36Mbps	-79
	12Mbps	-88	48Mbps	-74
	18Mbps	-86	54Mbps	-73
802.11n 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-79
	MCS1	-88	MCS5	-75
	MCS2	-86	MCS6	-72
	MCS3	-83	MCS7	-71
802.11ac 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-72

	MCS2	-86	**MCS7**	-71
	MCS3	-83	**MCS8**	-67
	MCS4	-79		
802.11ax 20MHz	**Data Rate**	**Spec.(dBm)**	**Data Rate**	**Spec.(dBm)**
	HE0	-90	**HE6**	-72
	HE1	-88	**HE7**	-71
	HE2	-86	**HE8**	-67
	HE3	-83	**HE9**	-64
	HE4	-79	**HE10**	-62
	HE5	-75	**HE11**	-61
Maximum Input Level	802.11a/n/ac/ax: -30 dBm			

3.3 6GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp=25°C

Feature	Description
WLAN Standard	IEEE 802.11ax & Wi-Fi compliant
Frequency Range	5925~7125MHz (6GHz U-NII5, U-NII6, U-NII-7, U-NII-8 Band)
Number of Channels	5925~6425MHz：6G1 ~ 6G93 6425~6525MHz：6G97 ~ 6G113 6525~6875MHz：6G117~6G181 6875~7125MHz：6G185~6G233
Modulation	802.11ax : OFDMA /1024-QAM、256-QAM、64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 2 dB

The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11ax 20MHz	**Frequency (MHz)**	**HE0~2**	**HE3**	**HE4**	**HE5**
	5925~6425	14.5	14	14	14
	6425~6525	14.5	14	14	14
	6525~6875	14	14	14	14
	6875~7125	13.5	13.5	13.5	13.5
	Frequency (MHz)	**HE6**	**HE7**	**HE8**	**HE9**
	5925~6425	14	13	11.5	10.5
	6425~6525	14	13	11.5	10.5
	6525~6875	14	13	11.5	10.5
	6875~7125	13	11	10.5	9.5
	Frequency (MHz)	**HE10**	**HE11**		
	5925~6425	9	9		
	6425~6525	9	9		
	6525~6875	9	9		
	6875~7125	8	8		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB, OFDM modulation PER ≦ 10%				
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-89	HE6	-71
	HE1	-86	HE7	-68
	HE2	-84	HE8	-66
	HE3	-83	HE9	-63
	HE4	-77	HE10	-61
	HE5	-74	HE11	-60
Maximum Input Level	802.11ax : -30dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

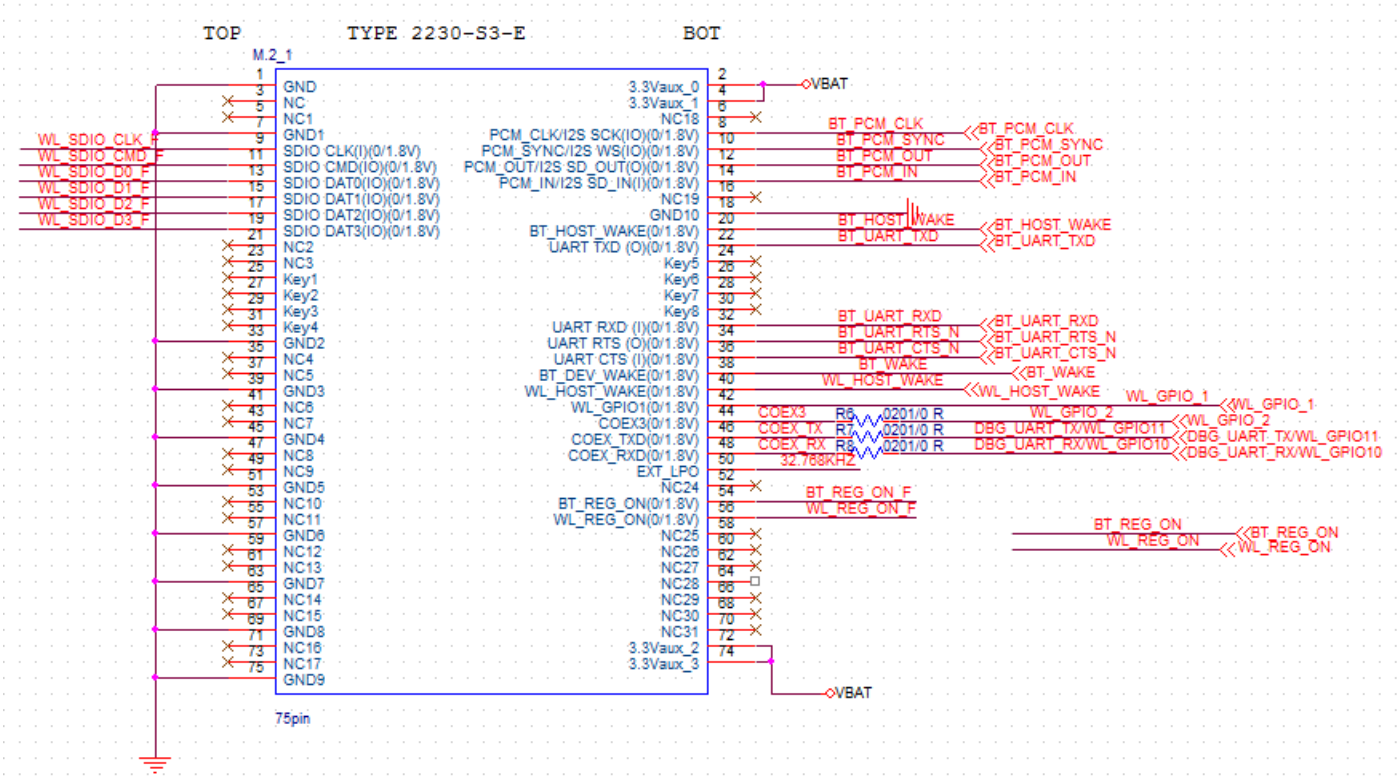
Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature	**Description**
General Specification	
Bluetooth Standard	BDR(1Mbps)、EDR(2、3Mbps)、LE(1Mbps)、2LE(2Mbps)
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic、40 channels for BLE
Modulation	GFSK, π/4-DQPSK, 8DPSK
RF Specification	
Output Power , tolerance ± 2.5 dB	
	CL1 (dBm)
BDR Output Power	7
EDR Output Power	7
BLE Output Power	7
Sensitivity, tolerance ± 2 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-87 dBm
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	-89 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-90 dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	π/4-DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note*：The Bluetooth BDR output power is able to be configured by firmware (hcd file).

5. Pin Definition

5.1 Pin Outline



5.2 Pin Assignment

NO	Name	Type	Description
		TOP	
1	GND	G	Ground connections
3	NC	—	No connect
5	NC	—	No connect
7	GND	G	Ground connections
9	SDIO_CLK	I	SDIO clock line
11	SDIO_CMD	I/O	SDIO command line
13	SDIO_DATA_0	I/O	SDIO data line 0
15	SDIO_DATA_1	I/O	SDIO data line 1
17	SDIO_DATA_2	I/O	SDIO data line 2
19	SDIO_DATA_3	I/O	SDIO data line 3
21	NC	—	No connect
23	NC	—	No connect
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
33	GND	G	Ground connections
35	NC	—	No connect
37	NC	—	No connect
39	GND	G	Ground connections
41	NC	—	No connect
43	NC	—	No connect
45	GND	G	Ground connections
47	NC	—	No connect
49	NC	—	No connect
51	GND	G	Ground connections
53	NC	—	No connect
55	NC	—	No connect
57	GND	G	Ground connections
59	NC	—	No connect
61	NC	—	No connect
63	GND	G	Ground connections
65	NC	—	No connect
67	NC	—	No connect

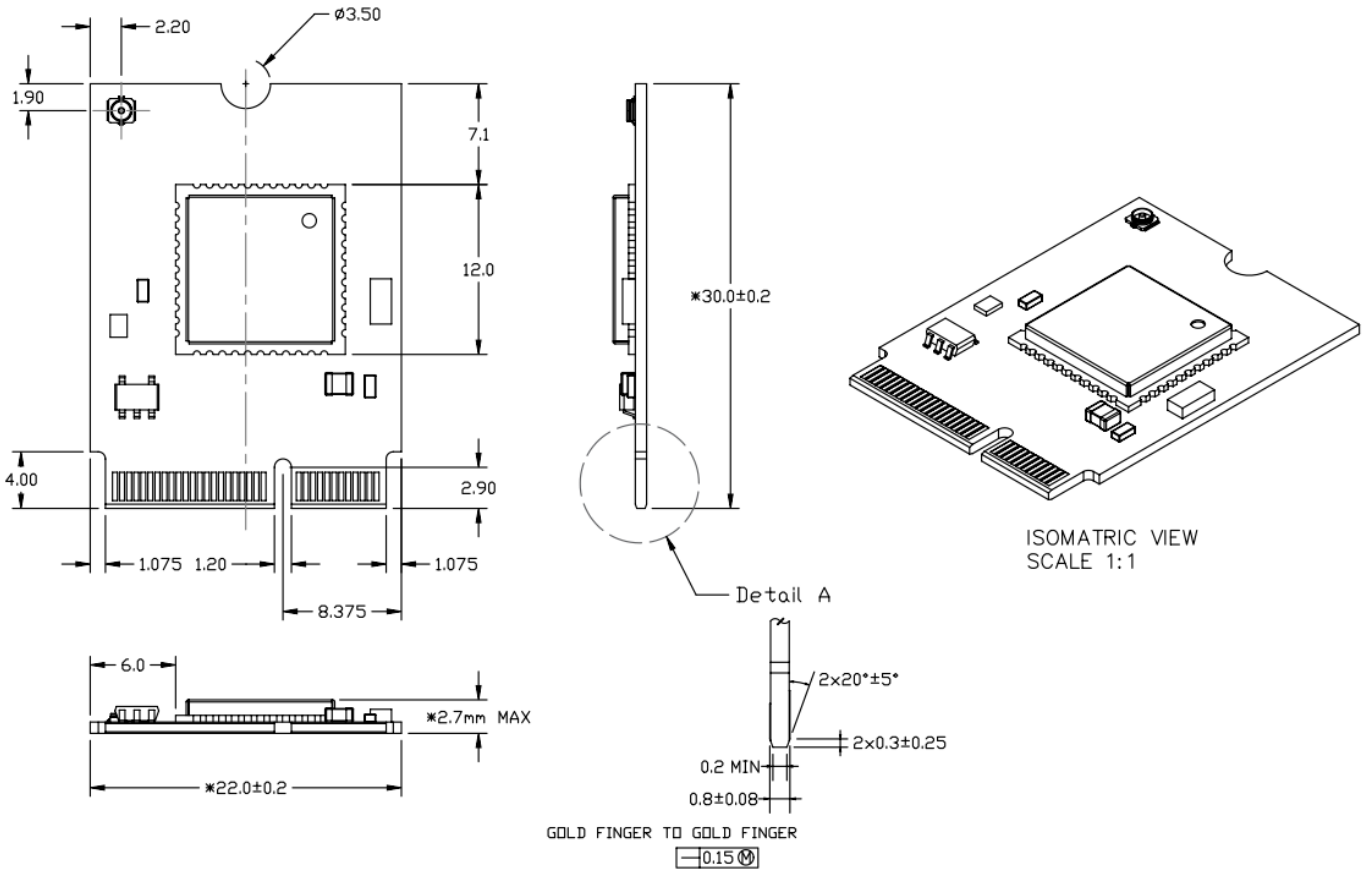
69	GND	G	Ground connections
71	NC	—	No connect
73	NC	—	No connect
75	GND	G	Ground connections
		BOTTOM	
2	3.3Vaux	P	VDD system power supply input
4	3.3Vaux	P	VDD system power supply input
6	NC	—	No connect
8	PCM_CLK (1.8V)	I/O	PCM clock
10	PCM_SYNC (1.8V)	I/O	PCM sync signal
12	PCM_OUT (1.8V)	O	PCM Data output
14	PCM_IN (1.8V)	I	PCM data input
16	NC	—	No connect
18	GND	G	Ground connections
20	BT_HOST_WAKE (1.8V)	O	Bluetooth wake up Host
22	UART_TXD (1.8V)	O	Bluetooth UART interface
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
32	UART_RXD (1.8V)	I	Bluetooth UART interface
34	UART_RTS_N (1.8V)	O	Bluetooth UART interface
36	UART_CTS_N (1.8V)	I	Bluetooth UART interface
38	BT_DEV_WAKE (1.8V)	I	HOST wake-up Bluetooth device
40	WL_HOST_WAKE (1.8V)	O	WLAN wake up HOST
42	WL_GPIO1(1.8V)	I/O	GPIO
44	WL_GPIO2(1.8V)	I/O	GPIO
46	GPIO11(1.8V)	I/O	UART Debug TX
48	GPIO10(1.8V)	I/O	UART Debug RX
50	NC	—	No connect
52	NC	—	No connect
54	BT_REG_ON (1.8V)	I	Used by PMU to power up or power down the internal module regulators used by the Bluetooth section.
56	WL_REG_ON (1.8V)	I	Used by PMU to power up or power down the internal module regulators used by the WLAN section.
58	NC	—	No connect
60	NC	—	No connect
62	NC	—	No connect
64	NC	—	No connect

66	NC	—	No connect
68	NC	—	No connect
70	NC	—	No connect
72	3.3Vaux	P	VDD system power supply input
74	3.3Vaux	P	VDD system power supply input

6. Dimensions

6.1 Module Dimensions

(Unit: mm)



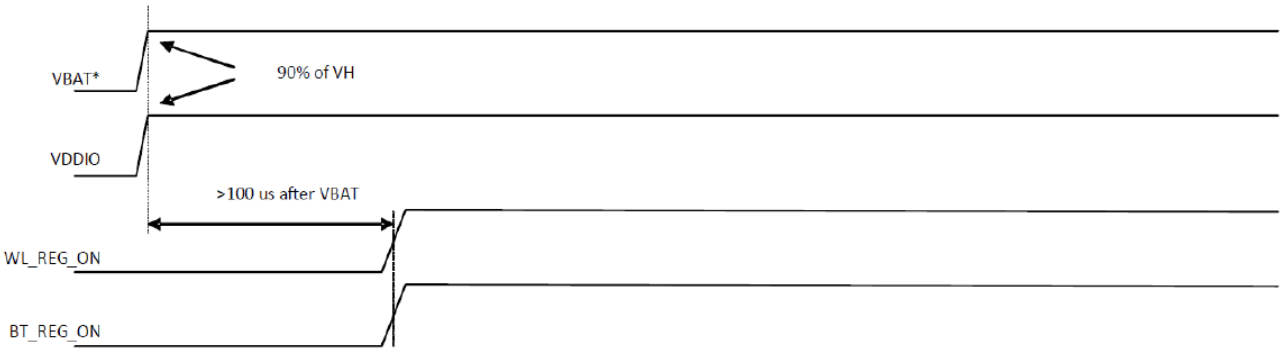
GENERAL TOLERANCE IS ±0.10mm
UNLESS OTHERWISE SPECIFIED

7. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

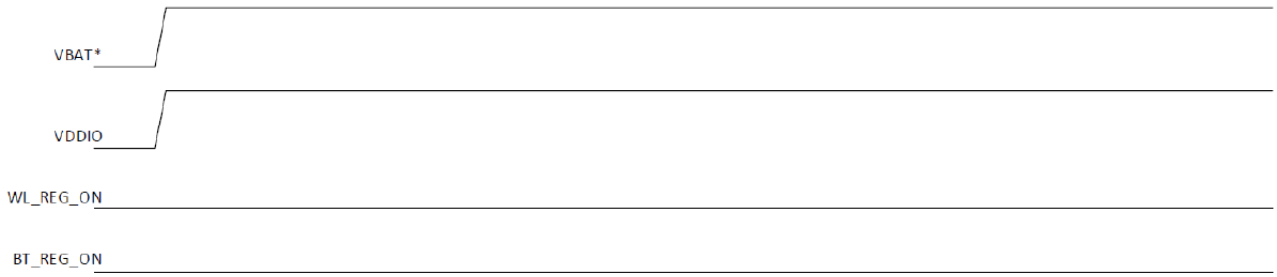
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

- WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



*Notes:
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO . VDDIO should NOT be present first or be held high before VBAT is high .

WLAN=ON, Bluetooth=ON

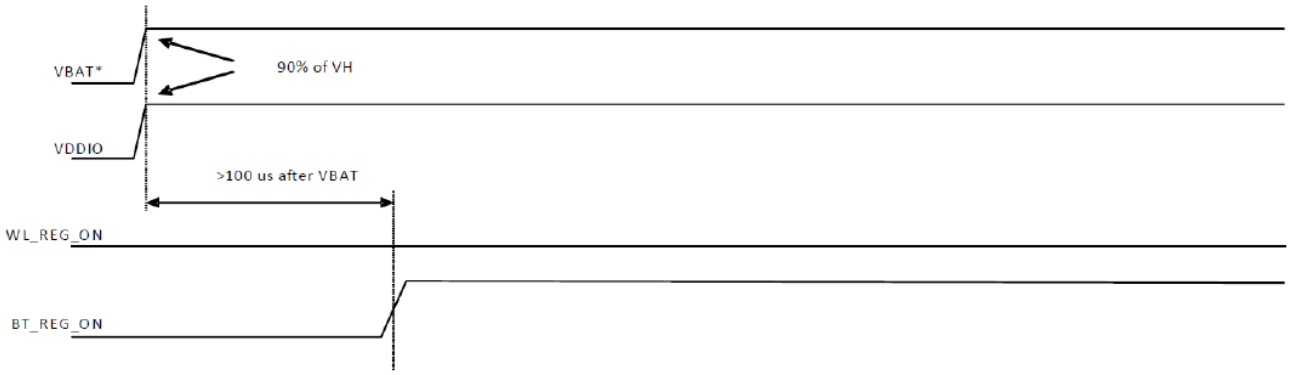


*Notes:
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=OFF, Bluetooth=OFF

***Notes:**
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 SDIO Interface Description

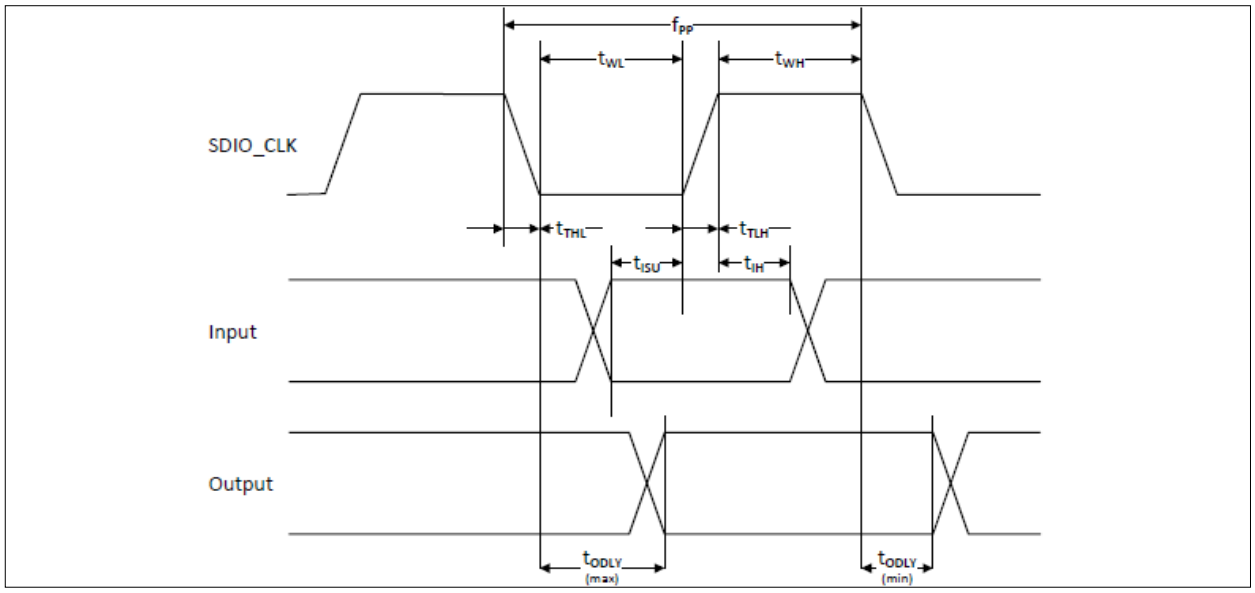
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps),SDR104(208MHz) and DDR50(50MHz, dual rates). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

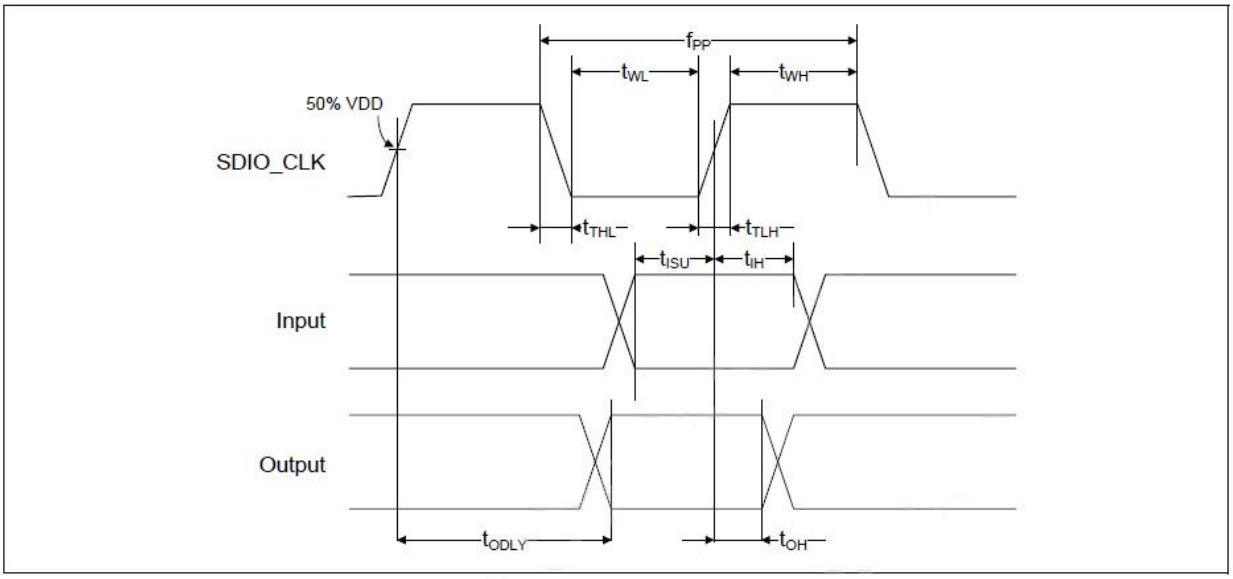
SDIO Default Mode Timing Diagram



Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO High Speed Mode Timing Diagram

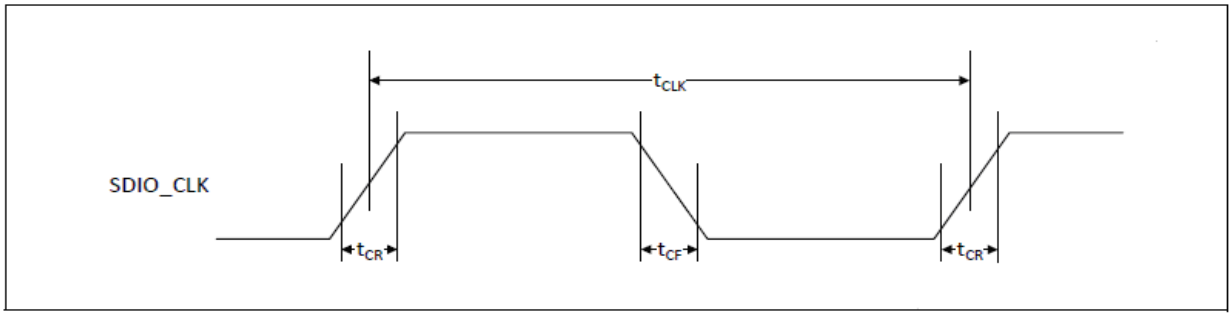


Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

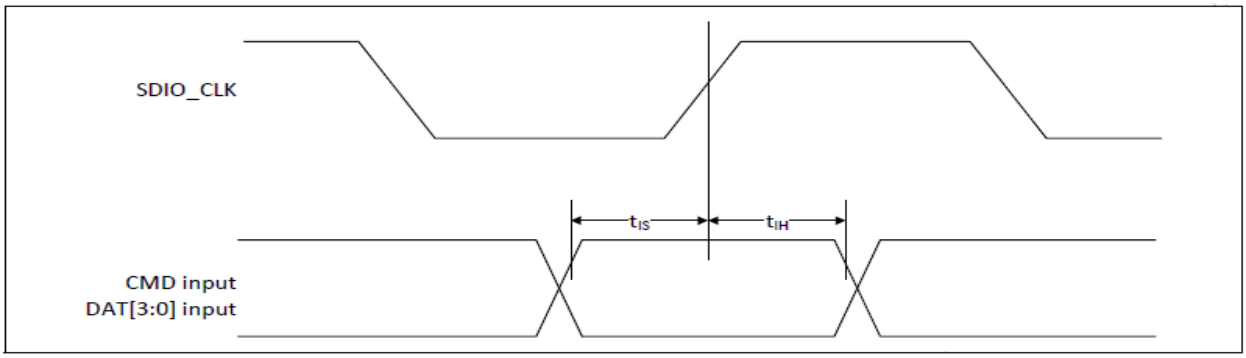
SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



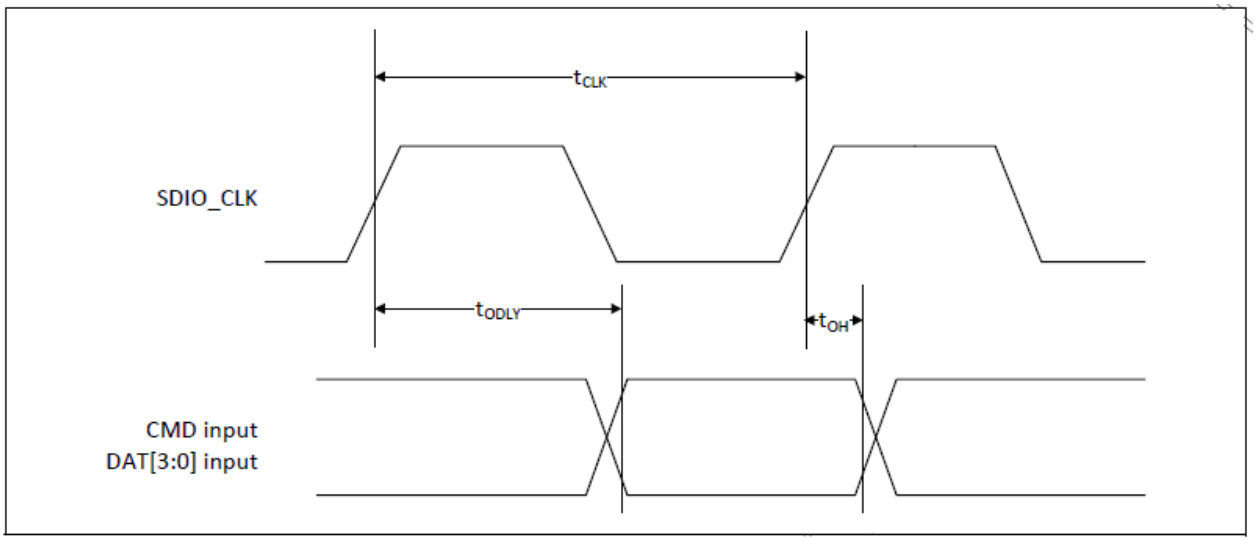
Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30	70	%	–

SDIO Bus Input timing (SDR Modes)



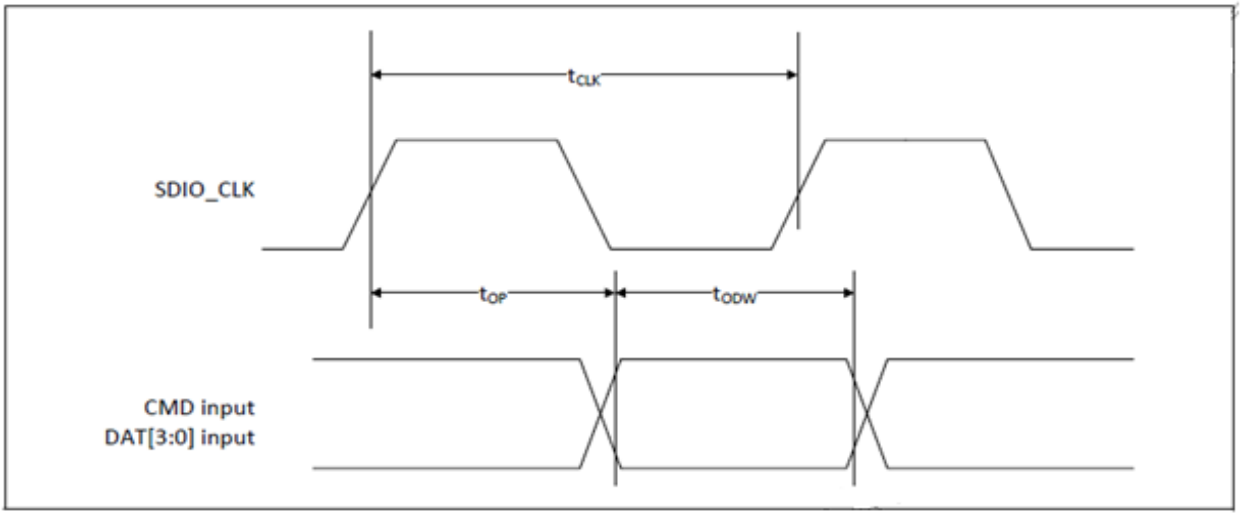
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

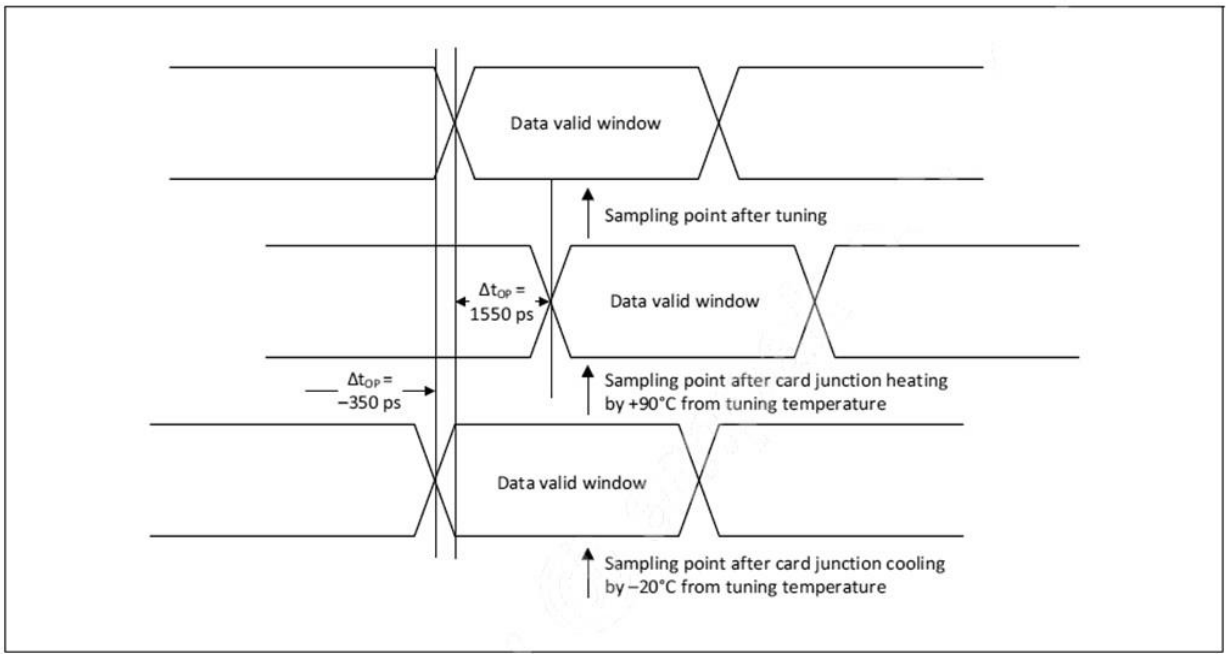
Card output timing (SDR Modes 100MHz to 208MHz)



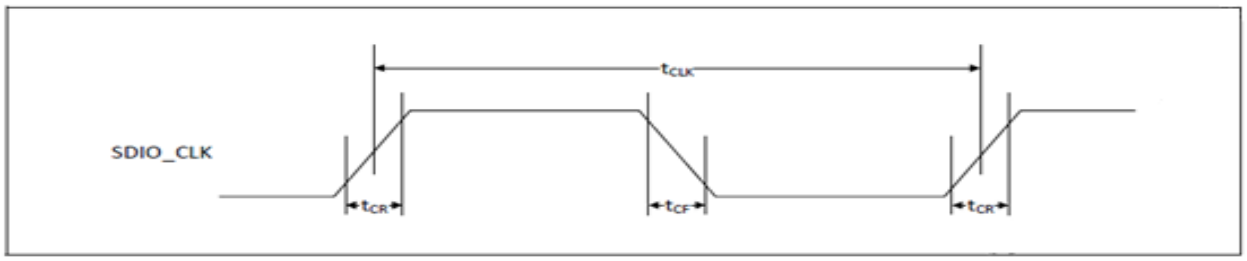
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	–350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	–	UI	t_{ODW}=2.88 ns @208 MHz

- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = –350 ps for junction temperature of Δt_{OP} = –20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = –20 to +125 degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

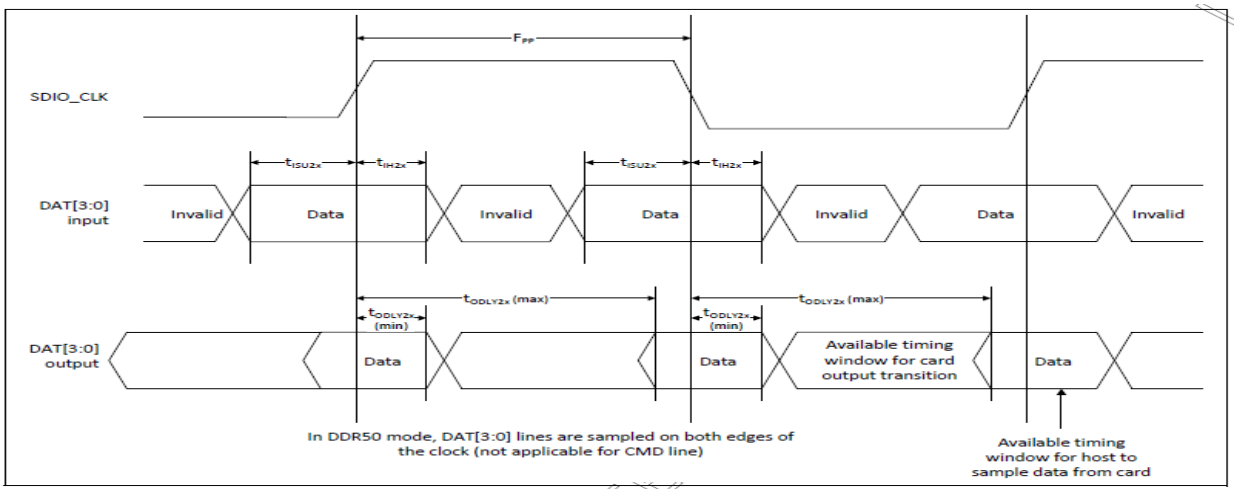


SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45	55	%	–

Data Timing



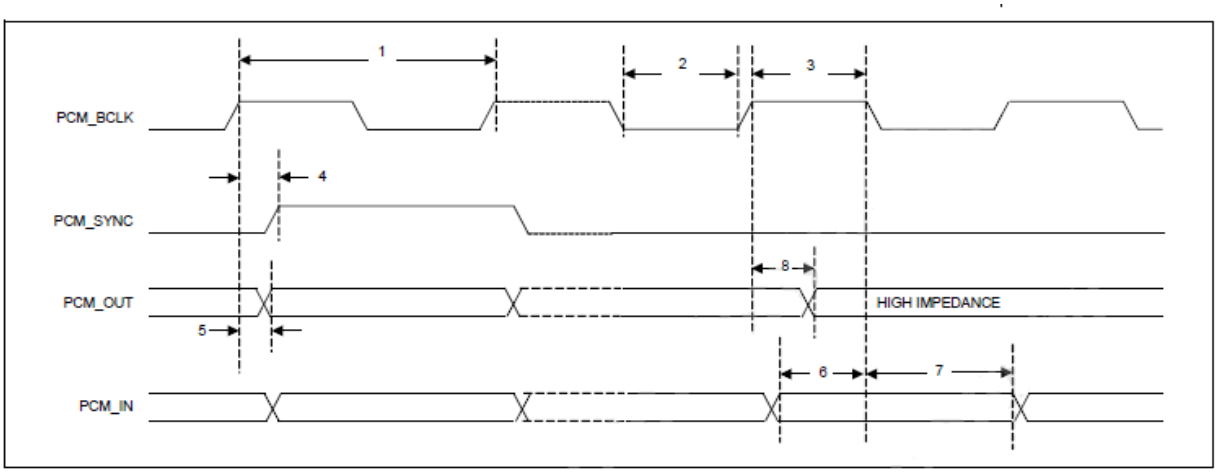
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

8.3 PCM Interface Description

The PCM Interface on the AP12612X_M2 can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP12612X_M2 generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP12612X_M2.The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

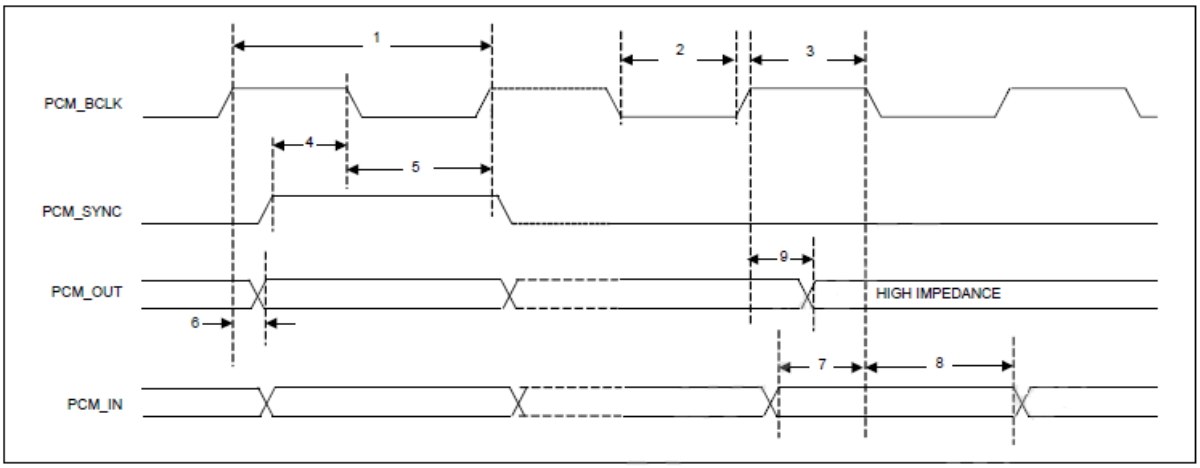


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

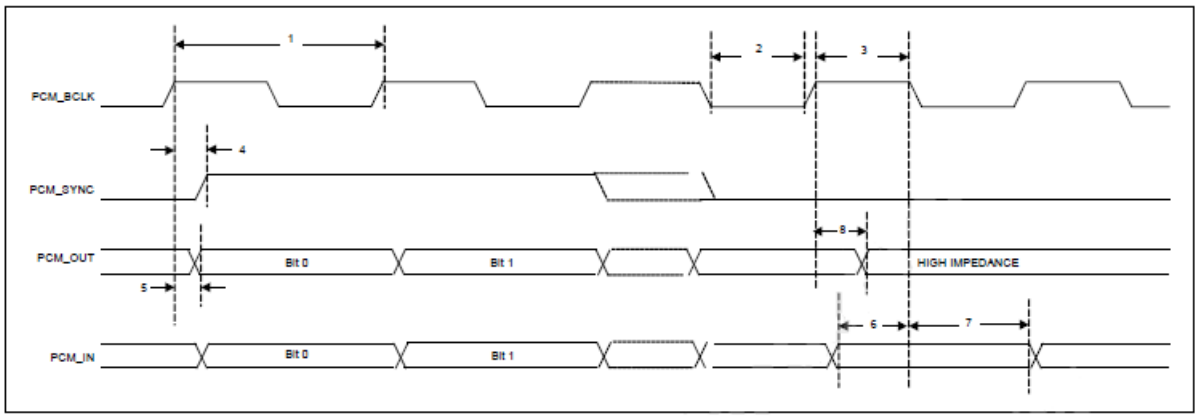


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

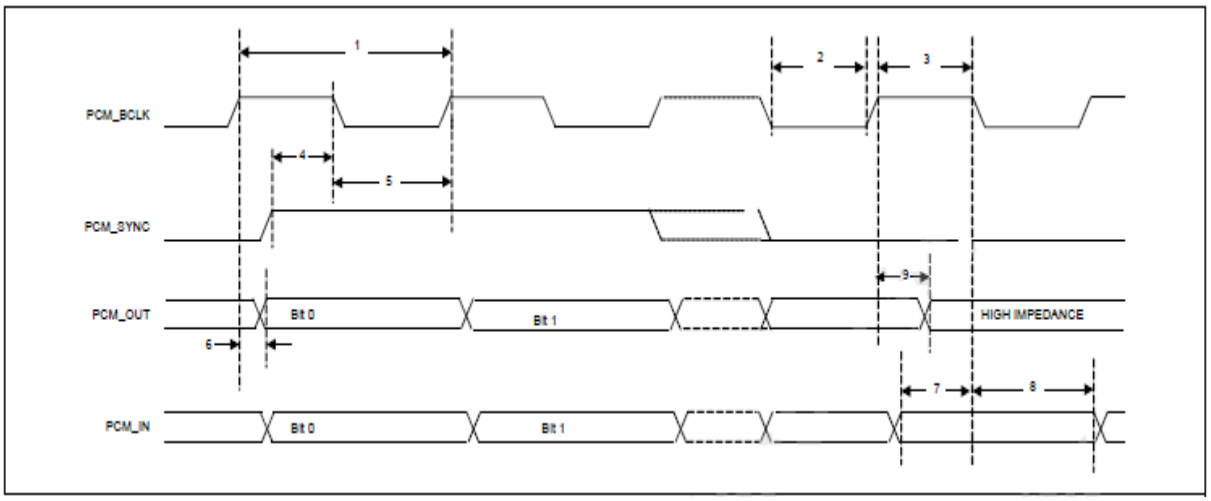


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

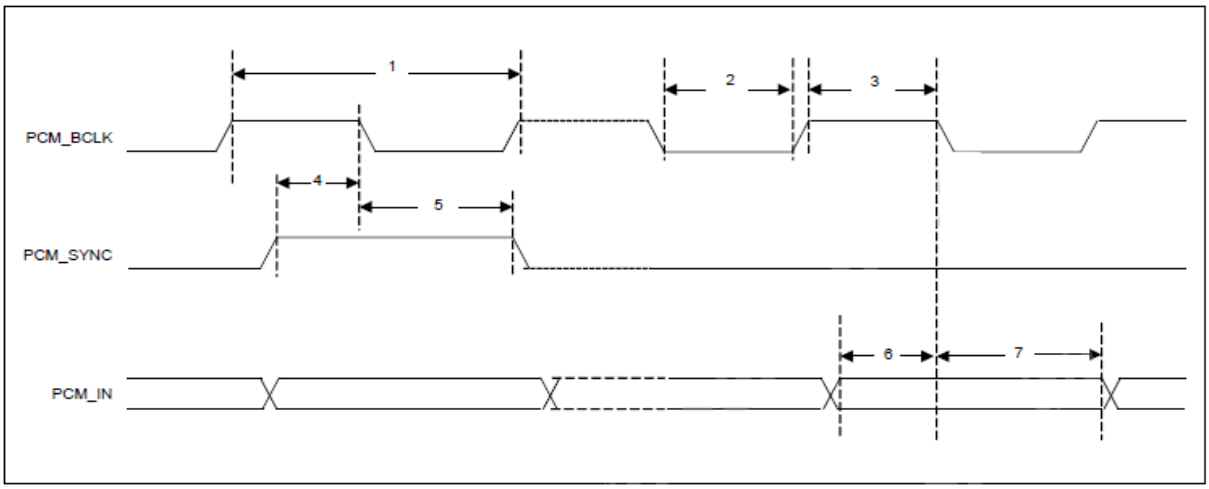


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

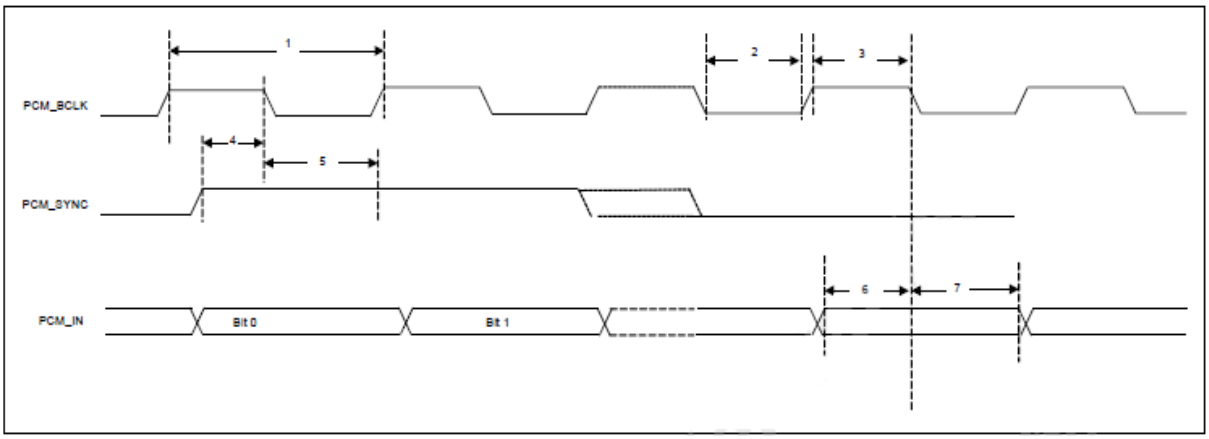


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

8.4 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

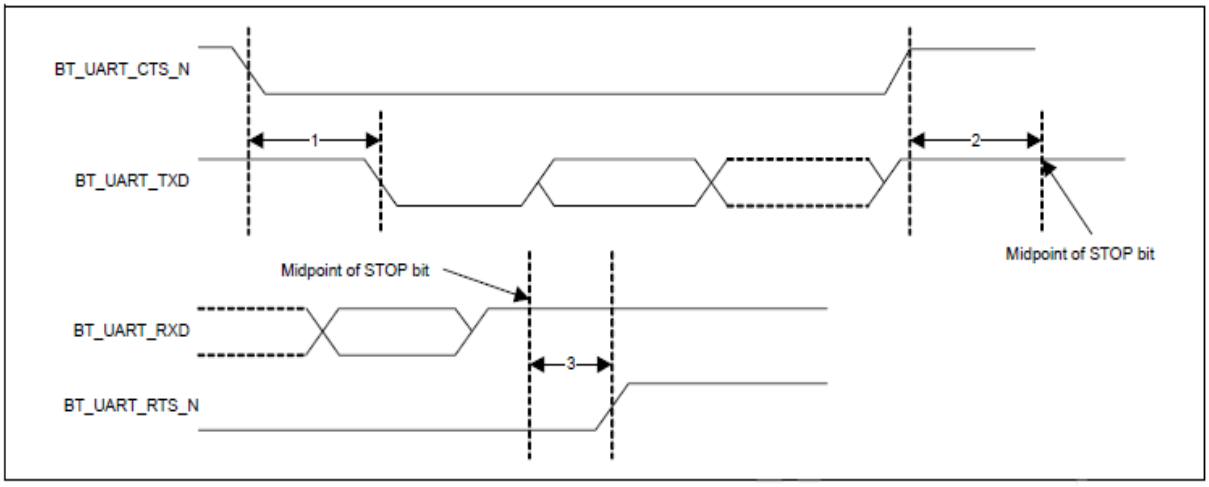
The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Example of Common Baud Rates

Desired Rate	Actual Rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing



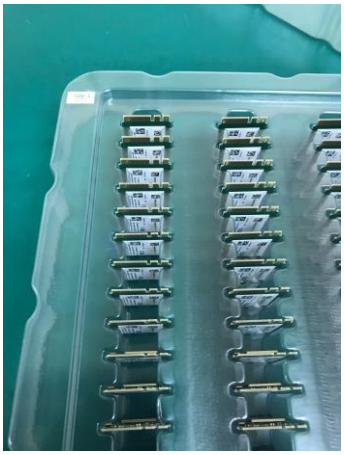
UART Timing Specifications

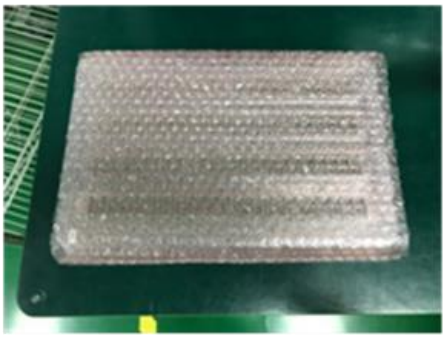
Ref	Characteristics	Min.	Typ.	Max.	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

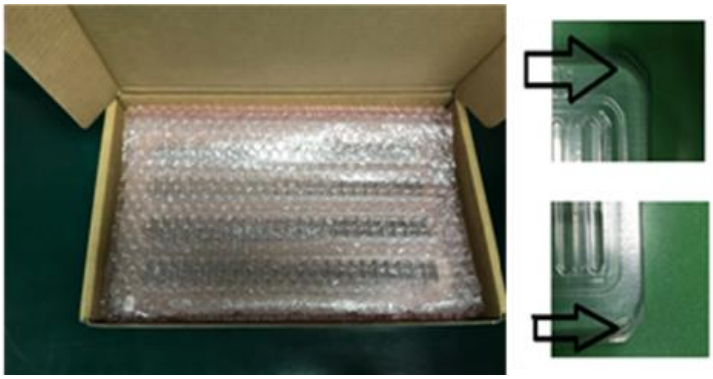
9. Package Information

9.1 Tray box

BOX : 100 PCS (100 PCS/Try)







9.2 Carton

Carton: 400 PCS (Box*4/Carton)