



正基科技股份有限公司

SPECIFICATION

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Customer APPROVED	
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正基科技股份有限公司



AP12275_M2 Data Sheet

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Revision

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0.2	2020/05/21	--Update RF Specification	Ares
0.3	2020/06/02	--Updated BT Specification	Ares
0.4	2020/08/12	--Update the RF block diagram	Ares
0.5	2020/09/22	--Update the RF block diagram	Ares
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0.7	2020/11/04	--Update the dimension	Ares
0.8	2021/02/19	--Add product label	Ares
0.9	2021/02/20	--Update package information	Ares
1.0	2021/03/31	--Add reference design and FCC power table	Ares
1.1	2021/04/20	--Update Pin Assignment	Jason
1.2	2021/05/07	--Update reference design	Richard
1.3	2021/06/25	--Update Bluetooth Specification	Richard
1.4	2022/10/27	--Modify 5GHz supported channel	Richard
1.5	2023/09/21	--Update Bluetooth Specification	Jason
1.6	2023/12/27	--Update Package Information and Add Ordering information	Kevin

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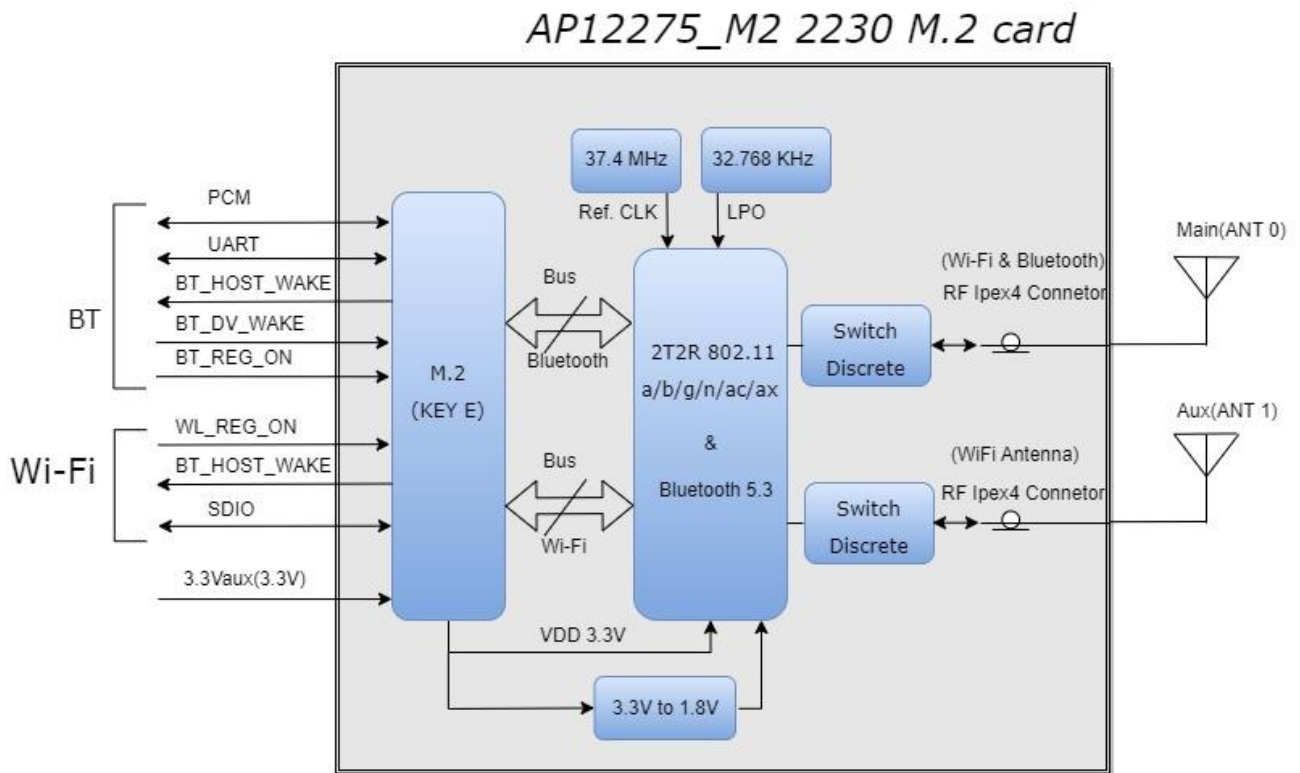
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1. Introduction

1.1 Overview

The AMPAK Technology® AP12275_M2 is a fully Wi-Fi and Bluetooth functionalities 2230 M.2 card (KEY E) with seamless roaming capabilities and advance security, also it could interact with different vendors' 802.11a/b/g/n/ac/ax 2x2 Access Points with MIMO standard and can accomplish up to speed of 1200Mbps with dual stream in 802.11ax to connect the wireless LAN. Furthermore AP12275_M2 included SDIO interface for Wi-Fi, UART/ PCM interface for Bluetooth

In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable devices.



1.2 Product Features

IEEE 802.11 Key Feature

- Lead Free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Dual-stream spatial multiplexing up to 1200 Mbps data rate.
- 20, 40, 80 MHz channels with optional SGI (1024 QAM modulation)
- IEEE 802.11ax beam forming
- Client MU-MIMO
- Supports standard SDIO v3.0, compatible with SDIO v2.0 HOST interfaces.

Bluetooth Key Feature

- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
 - Complies with Bluetooth Core Specification Version 5.3 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
 - Supports extended synchronous connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets.
 - Adaptive frequency hopping (AFH) for reducing radio frequency interference.
- A simplified block diagram of the module is depicted in the figure above.

2. General Specification

2.1 General Specification

Model Name	AP12275_M2
Product Description	2T2R 802.11 a/b/g/n/ac/ax Wi-Fi + BT 5.3 2230 M.2 card(KEY E)
Dimension	L x W : 30 x 22 mm (typical); H : 2.4 mm (max.)
WiFi Interface	SDIO V3.0/ 2.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 105°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and $3.2V < 3.3V_{aux} < 3.6V$ without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
3.3Vaux	Input supply Voltage	-0.5	4.5	V
WL_REG_ON	Used by PMU to power up or power down the internal regulators used by the WLAN section.	-0.5	2.07	V
BT_REG_ON	Used by PMU to power up or power down the internal regulators used by the Bluetooth section.			
WL_HOST_WAKE	WLAN device wake-up HOST			
BT_HOST_WAKE	Bluetooth device wake-up HOST			
BT_DEV_WAKE	HOST wake-up Bluetooth device			
Digital I/O	DC supply voltage for digital I/O			

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage.

Symbol	Condition	Minimum ESD Rating	Unit
ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/JESD22-A114	1.5	kV
ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	250	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: 3.3Vaux.

Voltage rails	Min.	Typ.	Max.	Unit
3.3Vaux	3.0	3.3	3.6	V
WL_REG_ON	1.62	1.8	1.98	V
BT_REG_ON				
WL_HOST_WAKE				
BT_HOST_WAKE				
BT_DEV_WAKE				

3.3Vaux current consumption 1200mA(Peak), when 3.3Vaux = 3.3V

Other Digital I/O Pins.

I/O Voltage = 1.8V	Min.	Max.	Unit
Input high voltage	1.17	NA	V
Input low voltage	NA	0.72	V
Output high voltage @ 2mA	1.4	NA	V
Output low voltage @ 2mA	NA	0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : 3.3V_{aux}=3.3V; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11 b/g/n/ax & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz：Ch1 ~ Ch13			
Modulation		802.11b：DQPSK、DBPSK、CCK 802.11g/n：OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ax：OFDMA /256-QAM、64-QAM、16-QAM、QPSK、BPSK			
Output Power , tolerance ± 1.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	17.5	17.5	17.5	17.5	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	12	12	12	12	12
	54Mbps				
	12				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	12	12	12	12	12
	MCS7				
	12				
802.11ax 20MHz	HE0~2	HE3	HE4	HE5	HE6
	12	12	12	12	12
	HE7	HE8	HE9		
	12	12	12		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB				
CCK modulation PER $\leq 8\%$ 、 OFDM modulation PER $\leq 10\%$				
802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-96		
	2Mbps	-92		
	5.5Mbps	-90		
	11Mbps	-88		

802.11g SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-92	24Mbps	-84
	9Mbps	-91	36Mbps	-81
	12Mbps	-90	48Mbps	-77
	18Mbps	-87	54Mbps	-75
802.11g MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-94	24Mbps	-86
	9Mbps	-93	36Mbps	-83
	12Mbps	-92	48Mbps	-80
	18Mbps	-89	54Mbps	-77
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS4	-80
	MCS1	-88	MCS5	-78
	MCS2	-86	MCS6	-75
	MCS3	-83	MCS7	-74
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-92	MCS5	-79
	MCS1	-91	MCS6	-77
	MCS2	-89	MCS7	-75
	MCS3	-86	MCS8	-71
	MCS4	-82	MCS15	-72
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-92	HE6	-75
	HE1	-88	HE7	-75
	HE2	-86	HE8	-71
	HE3	-83	HE9	-69
	HE4	-80		
	HE5	-78		
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n/ax : -20 dBm			

3.2 5GHz RF Specification

Conditions : 3.3V_{aux}=3.3V; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac/ax & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz (5GHz UNII Band)			
Number of Channels		5.15~5.35GHz : Ch36 ~ Ch64 5.47~5.725GHz : Ch100 ~ Ch144 5.725~5.85GHz : Ch149 ~ Ch165			
Modulation		802.11a : OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n : OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac : OFDM /256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ax : OFDMA /1024-QAM 、 256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	14	14	14	14
	5470~5725	14.5	14.5	14.5	14.5
	5725~5845	14.5	14.5	14.5	14.5
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	14	14		
	5470~5725	14.5	14.5		
	5725~5845	14.5	14.5		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	14	14	14	14
	5470~5725	14.5	14.5	14.5	14.5
	5725~5845	14.5	14.5	14.5	14.5
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	13	13		
	5470~5725	13.5	13.5		
	5725~5845	13.5	13.5		

802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	11	11	11	11
	5470~5725	11	11	11	11
	5725~5845	11	11	11	11
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	11	11		
	5470~5725	11	11		
	5725~5845	11	11		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	14	14	14	14
	5470~5725	14.5	14.5	14.5	14.5
	5725~5845	14.5	14.5	14.5	14.5
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	13	13	10	
	5470~5725	13.5	13.5	10	
	5725~5845	13.5	13.5	10	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	11	11	11	11
	5470~5725	11	11	11	11
	5725~5845	11	11	11	11
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	11	11	10	9
	5470~5725	11	11	10	9
	5725~5845	11	11	10	9
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	11	11	11	11
	5470~5725	11	11	11	11
	5725~5845	11	11	11	11
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	11	11	9	9
	5470~5725	11	11	9	9
	5725~5845	11	11	9	9
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	14	14	14	14
	5470~5725	14.5	14.5	14.5	14.5
	5725~5845	14.5	14.5	14.5	14.5

802.11ax 20MHz	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	13	13	10	10
	5470~5725	13.5	13.5	10	10
	5725~5845	13.5	13.5	10	10
	Frequency (MHz)	HE10	HE11		
	5150~5350	9	9		
	5470~5725	9	9		
	5725~5845	9	9		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	11	11	11	11
	5470~5725	11	11	11	11
	5725~5845	11	11	11	11
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	11	11	10	9
	5470~5725	11	11	10	9
	5725~5845	11	11	10	9
	Frequency (MHz)	HE10	HE11		
	5150~5350	7	7		
	5470~5725	7	7		
	5725~5845	7	7		
802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	11	11	11	11
	5470~5725	11	11	11	11
	5725~5845	11	11	11	11
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	11	11	9	9
	5470~5725	11	11	9	9
	5725~5845	11	11	9	9
	Frequency (MHz)	HE10	HE11		
	5150~5350	7	7		
	5470~5725	7	7		
	5725~5845	7	7		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB				
CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$				
802.11a SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-89	24Mbps	-82
	9Mbps	-88	36Mbps	-79
	12Mbps	-87	48Mbps	-74
	18Mbps	-85	54Mbps	-72
802.11a MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-85
	9Mbps	-90	36Mbps	-82
	12Mbps	-89	48Mbps	-77
	18Mbps	-88	54Mbps	-76
802.11n_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS4	-78
	MCS1	-87	MCS5	-75
	MCS2	-85	MCS6	-72
	MCS3	-82	MCS7	-70
802.11n_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-91	MCS5	-77
	MCS1	-90	MCS6	-75
	MCS2	-88	MCS7	-74
	MCS3	-85	MCS8	-88
	MCS4	-81	MCS15	-69
802.11n_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-87	MCS4	-76
	MCS1	-85	MCS5	-71
	MCS2	-82	MCS6	-69
	MCS3	-79	MCS7	-67
802.11n_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-87	MCS5	-74
	MCS1	-87	MCS6	-72
	MCS2	-85	MCS7	-70
	MCS3	-82	MCS8	-85
	MCS4	-78	MCS15	-66

802.11ac_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-89	MCS5	-74
	MCS1	-87	MCS6	-72
	MCS2	-85	MCS7	-69
	MCS3	-82	MCS8	-67
	MCS4	-78		
802.11ac_20MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-91	MCS6,NSS=1	-75
	MCS1,NSS=1	-90	MCS7,NSS=1	-74
	MCS2,NSS=1	-87	MCS8,NSS=1	-71
	MCS3,NSS=1	-84	MCS0,NSS=2	-87
	MCS4,NSS=1	-81	MCS8,NSS=2	-64
	MCS5,NSS=1	-76		
802.11ac_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-87	MCS5	-71
	MCS1	-85	MCS6	-69
	MCS2	-82	MCS7	-68
	MCS3	-79	MCS8	-64
	MCS4	-75	MCS9	-63
802.11ac_40MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-89	MCS6,NSS=1	-72
	MCS1,NSS=1	-87	MCS7,NSS=1	-71
	MCS2,NSS=1	-85	MCS8,NSS=1	-67
	MCS3,NSS=1	-81	MCS9,NSS=1	-65
	MCS4,NSS=1	-78	MCS0,NSS=2	-85
	MCS5,NSS=1	-76	MCS9,NSS=2	-59
802.11ac_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-84	MCS5	-67
	MCS1	-81	MCS6	-66
	MCS2	-78	MCS7	-64
	MCS3	-75	MCS8	-61
	MCS4	-72	MCS9	-60

802.11ac_80MHz MIMO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0,NSS=1	-86	MCS6,NSS=1	-69
	MCS1,NSS=1	-84	MCS7,NSS=1	-67
	MCS2,NSS=1	-81	MCS8,NSS=1	-65
	MCS3,NSS=1	-78	MCS9,NSS=1	-62
	MCS4,NSS=1	-75	MCS0,NSS=2	-82
	MCS5,NSS=1	-70	MCS9,NSS=2	-57
802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-89	HE6	-72
	HE1	-87	HE7	-69
	HE2	-85	HE8	-67
	HE3	-82	HE9	-63
	HE4	-78	HE10	-58
	HE5	-74	HE11	-56
802.11ax_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-87	HE6	-69
	HE1	-85	HE7	-68
	HE2	-82	HE8	-64
	HE3	-79	HE9	-63
	HE4	-75	HE10	-59
	HE5	-71	HE11	-54
802.11ax_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-84	HE6	-66
	HE1	-81	HE7	-64
	HE2	-78	HE8	-61
	HE3	-75	HE9	-60
	HE4	-72	HE10	-54
	HE5	-67	HE11	-50
Maximum Input Level	802.11a/n/ac/ax : -30 dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : 3.3V_{Vaux}=3.3V; Temp:25°C

Feature	Description
General Specification	
Bluetooth Standard	BDR、EDR(1Mbps & 2Mbps)、LE(1Mbps)、2LE(2Mbps)
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic、40 channels for BLE
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK
RF Specification	
Output Power, tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	8
EDR Output Power	6
BLE Output Power	7
Sensitivity, tolerance ± 2 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-88 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-91 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-85 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-91dBm
Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).

5. Pin Definition

5.1 Pin Outline

M.2_2			
1		2	
3	GND	3.3Vaux	4
5	NC	3.3Vaux	6
7	NC	NC	8
9	GND	PCM_CLK/I2S SCK(IO)(0/1.8V)	10
11	SDIO CLK(I)(0/1.8V)	PCM_SYNC/I2S WS(IO)(0/1.8V)	12
13	SDIO CMD(IO)(0/1.8V)	PCM_OUT/I2S SD_OUT(O)(0/1.8V)	14
15	SDIO DAT0(IO)(0/1.8V)	PCM_IN/I2S SD_IN(I)(0/1.8V)	16
17	SDIO DAT1(IO)(0/1.8V)	NC	18
19	SDIO DAT2(IO)(0/1.8V)	GND	20
21	SDIO DAT3(IO)(0/1.8V)	BT_HOST_WAKE(0/1.8V)	22
23	NC	UART TXD (O)(0/1.8V)	24
25	NC	Key	26
27	Key	Key	28
29	Key	Key	30
31	Key	Key	32
33	Key	UART RXD (I)(0/1.8V)	34
35	GND	UART RTS (O)(0/1.8V)	36
37	NC	UART CTS (I)(0/1.8V)	38
39	NC	BT_DEV_WAKE(0/1.8V)	40
41	GND	WL_HOST_WAKE(0/1.8V)	42
43	NC	NC	44
45	NC	NC	46
47	GND	NC	48
49	NC	NC	50
51	NC	EXT_LPO	52
53	GND	NC	54
55	NC	BT_REG_ON(0/1.8V)	56
57	NC	WL_REG_ON(0/1.8V)	58
59	GND	NC	60
61	NC	NC	62
63	NC	NC	64
65	GND	NC	66
67	NC	NC	68
69	NC	NC	70
71	GND	NC	72
73	NC	3.3Vaux	74
75	NC	3.3Vaux	
	GND		

75pin

5.1 Pin Assignment

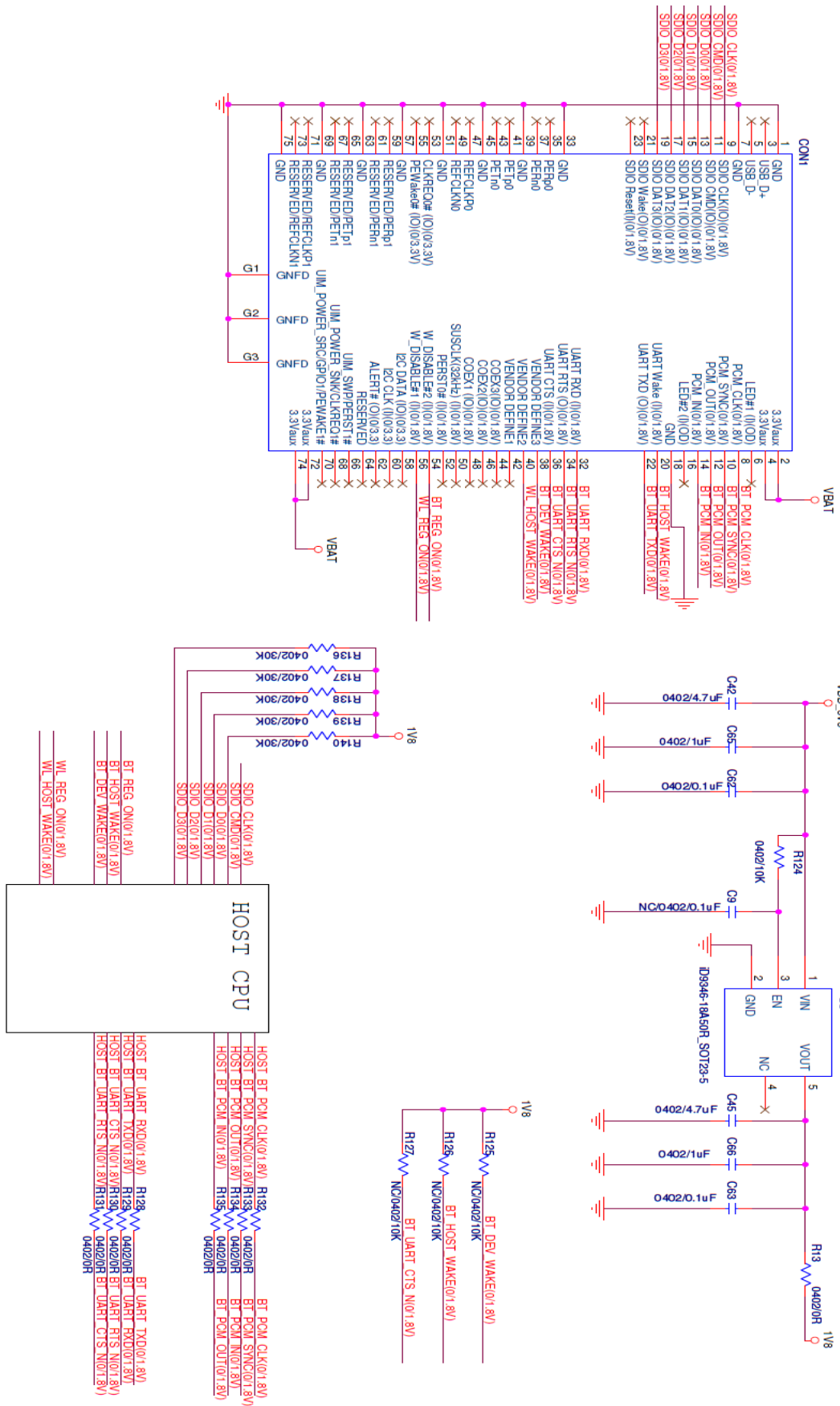
NO	Name	Type	Description
TOP			
1	GND	G	Ground connections
3	NC	—	No connect
5	NC	—	No connect
7	GND	G	Ground connections
9	SDIO_CLK	I	SDIO clock line
11	SDIO_CMD	I/O	SDIO command line
13	SDIO_DATA_0	I/O	SDIO data line 0
15	SDIO_DATA_1	I/O	SDIO data line 1
17	SDIO_DATA_2	I/O	SDIO data line 2
19	SDIO_DATA_3	I/O	SDIO data line 3
21	NC	—	No connect
23	NC	—	No connect
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
33	GND	G	Ground connections
35	NC	—	No connect
37	NC	—	No connect
39	GND	G	Ground connections
41	NC	—	No connect
43	NC	—	No connect
45	GND	G	Ground connections
47	NC	—	No connect
49	NC	—	No connect
51	GND	G	Ground connections
53	NC	—	No connect
55	NC	—	No connect
57	GND	G	Ground connections
59	NC	—	No connect
61	NC	—	No connect
63	GND	G	Ground connections
65	NC	—	No connect

67	NC	—	No connect
69	GND	G	Ground connections
71	NC	—	No connect
73	NC	—	No connect
75	GND	G	Ground connections
BOTTOM			
2	3.3Vaux	P	VDD system power supply input
4	3.3Vaux	P	VDD system power supply input
6	NC	—	No connect
8	PCM_CLK (1.8V)	I/O	PCM clock
10	PCM_SYNC (1.8V)	I/O	PCM sync signal
12	PCM_OUT (1.8V)	O	PCM Data output
14	PCM_IN (1.8V)	I	PCM data input
16	NC	—	No connect
18	GND	G	Ground connections
20	BT_HOST_WAKE (1.8V)	O	Bluetooth wake up Host
22	UART_TXD (1.8V)	O	Bluetooth UART interface
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
	Module Key	—	Mechanical Key
32	UART_RXD (1.8V)	I	Bluetooth UART interface
34	UART_RTS_N (1.8V)	O	Bluetooth UART interface
36	UART_CTS_N (1.8V)	I	Bluetooth UART interface
38	BT_DEV_WAKE (1.8V)	I	HOST wake-up Bluetooth device
40	WL_HOST_WAKE (1.8V)	O	WLAN wake up HOST
42	NC	—	No connect
44	NC	—	No connect
46	NC	—	No connect
48	NC	—	No connect
50	NC	—	No connect
52	NC	—	No connect
54	BT_REG_ON (1.8V)	I	Used by PMU to power up or power down the internal module regulators used by the Bluetooth section.
56	WL_REG_ON (1.8V)	I	Used by PMU to power up or power down the internal module regulators used by the WLAN section.
58	NC	—	No connect

60	NC	—	No connect
62	NC	—	No connect
64	NC	—	No connect
66	NC	—	No connect
68	NC	—	No connect
70	NC	—	No connect
72	3.3Vaux	P	VDD system power supply input
74	3.3Vaux	P	VDD system power supply input

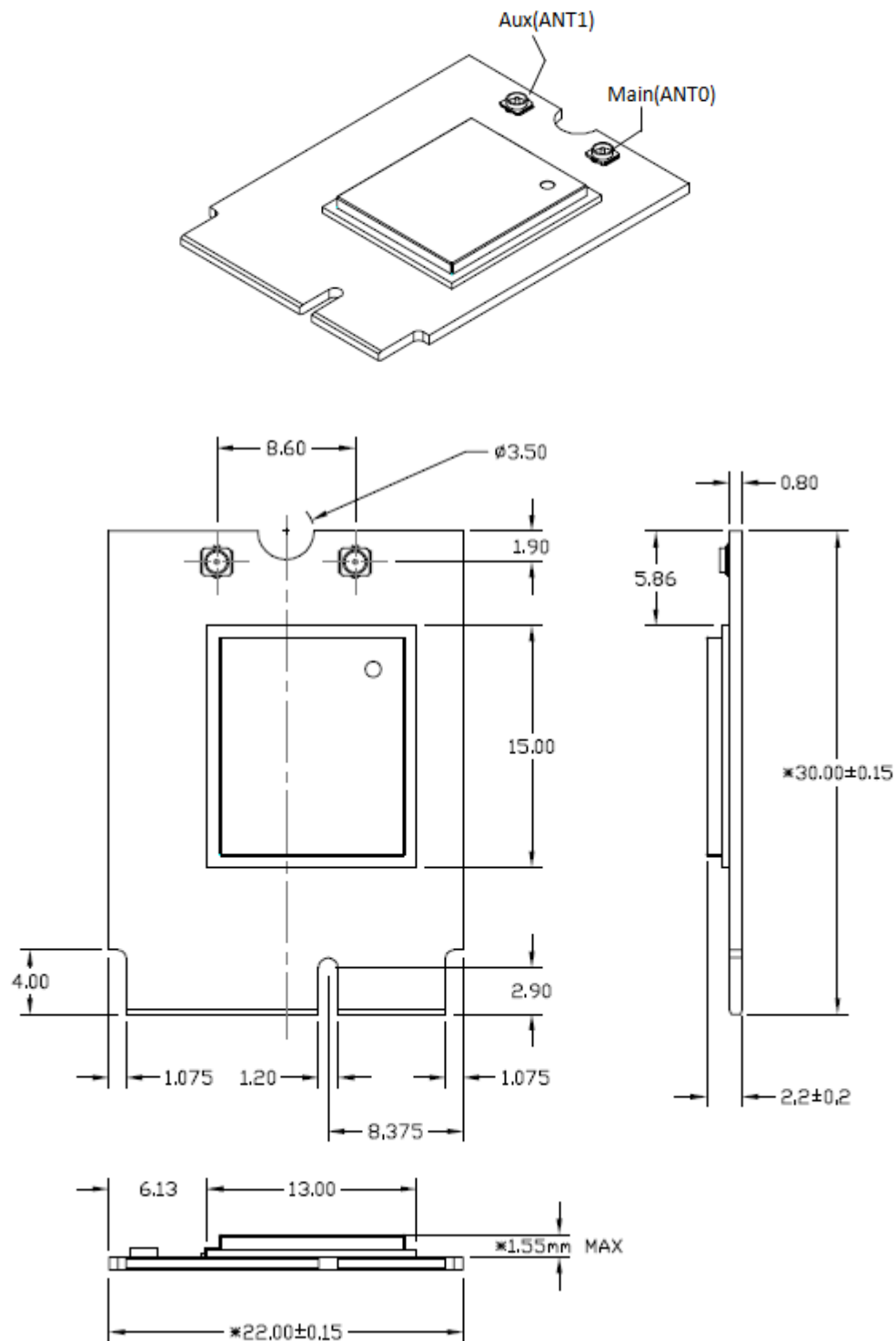
6. Reference Design

SDIO Based Module Solution Pinout (Module Key E)



7. Dimensions

7.1 Module Dimensions



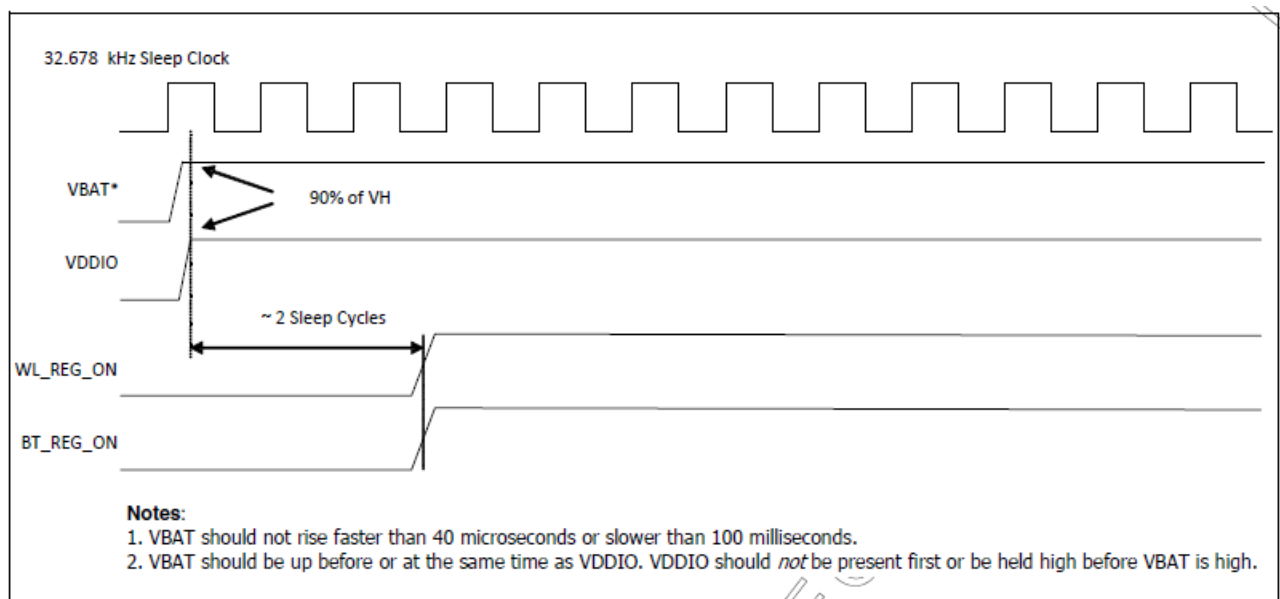
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

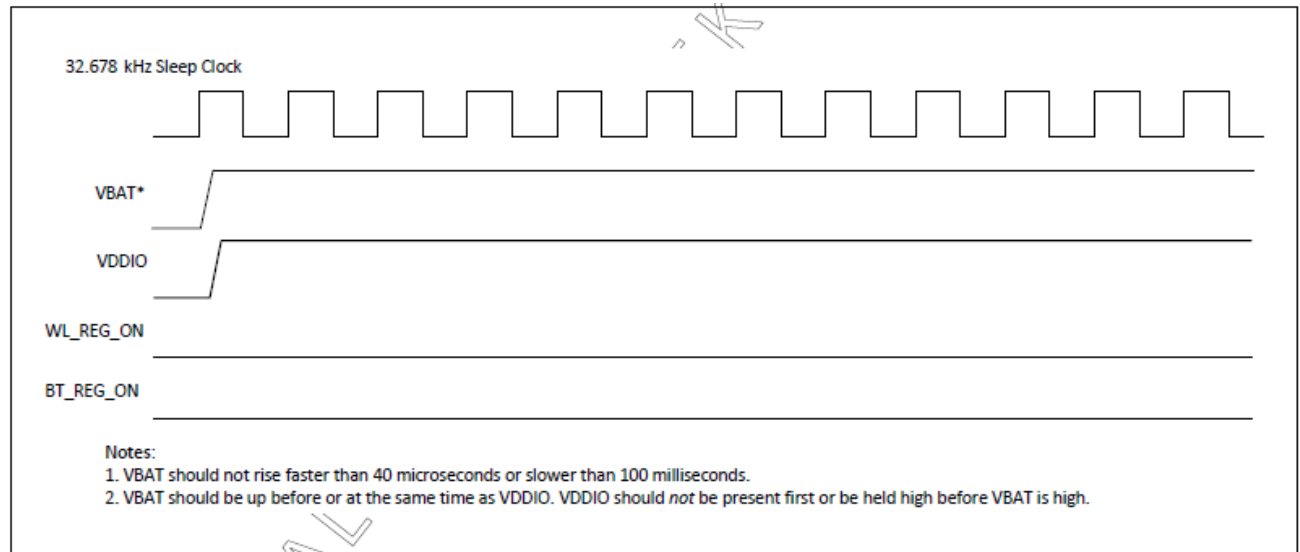
The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

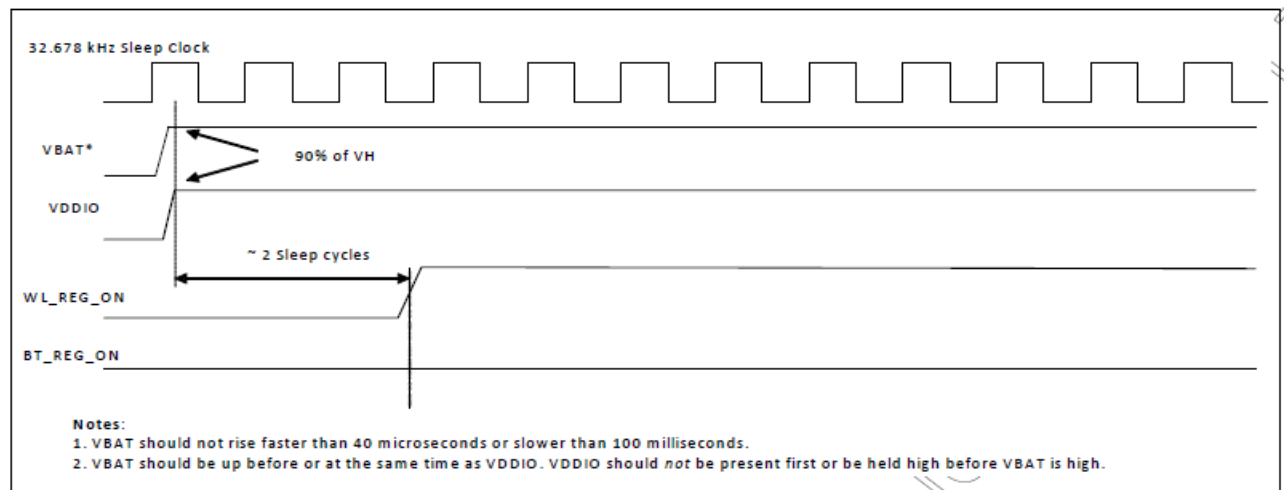
- **WL_REG_ON:** Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_REG_ON:** Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



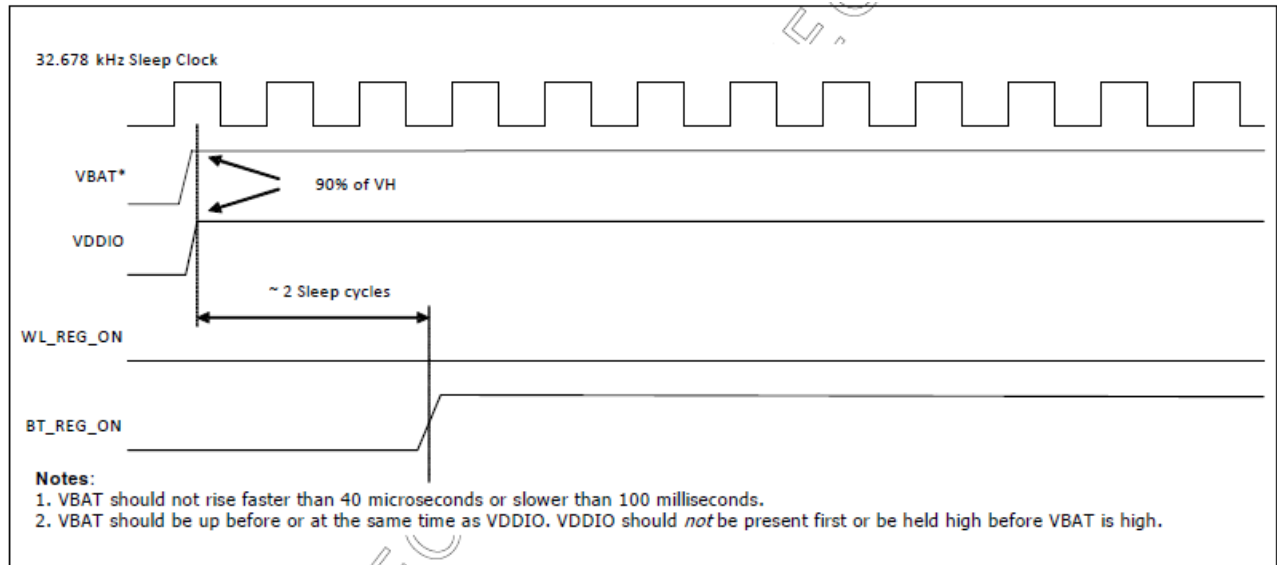
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 SDIO Interface Description

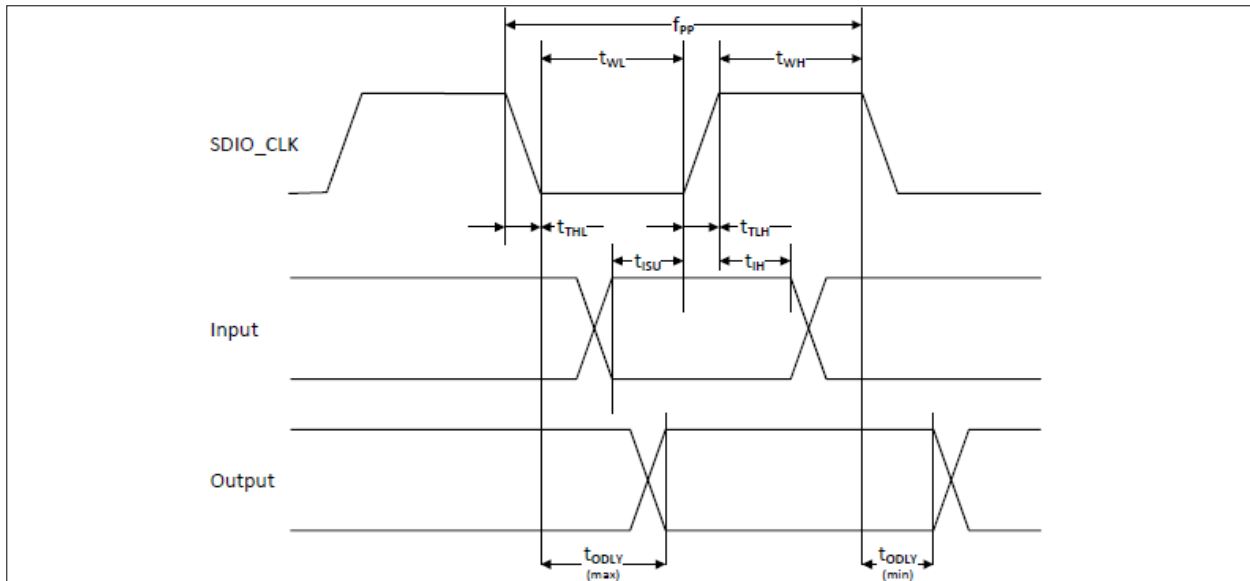
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps), SDR104(208MHz) and DDR50(50MHz, dual rates). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

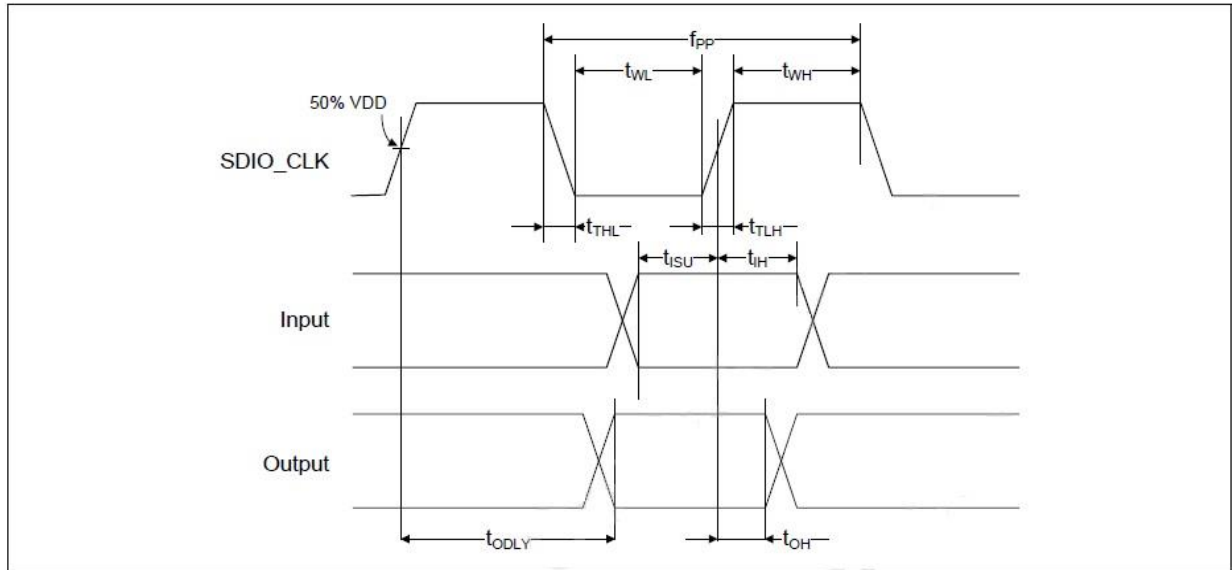
SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

- a. Timing is based on $CL \leq 40pF$ load on CMD and Data.
 b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

SDIO High Speed Mode Timing Diagram



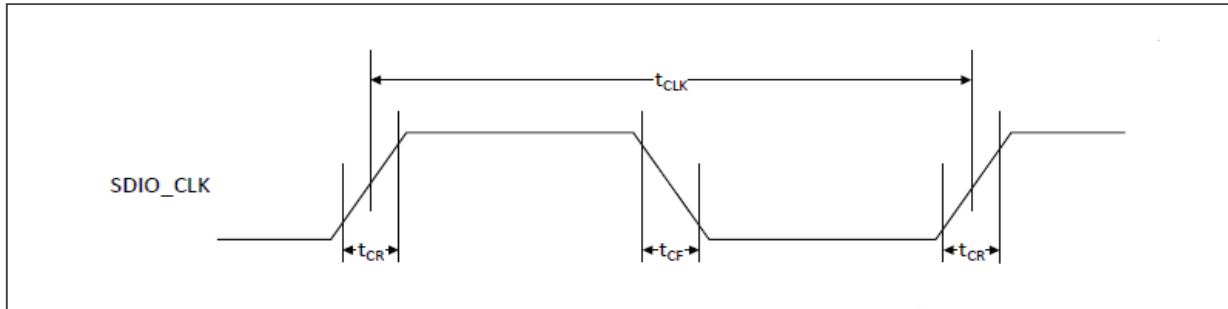
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer Mode	f_{pp}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on $CL \leq 40$ pF load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

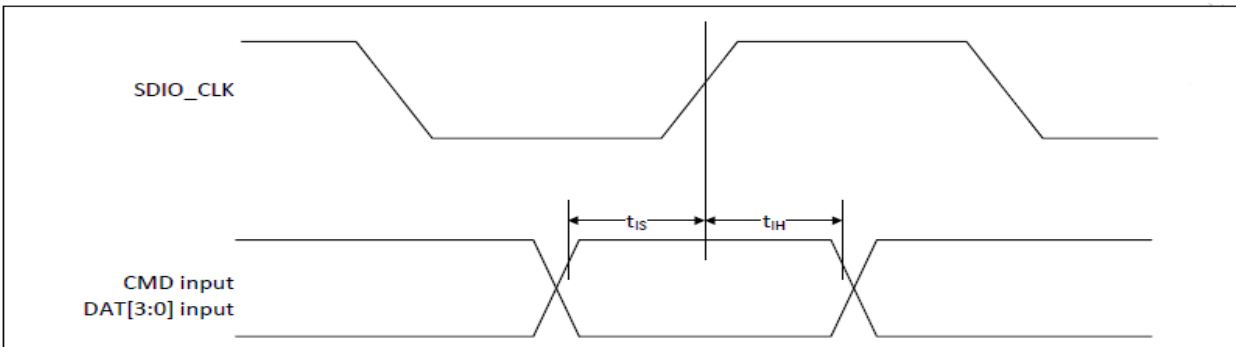
SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



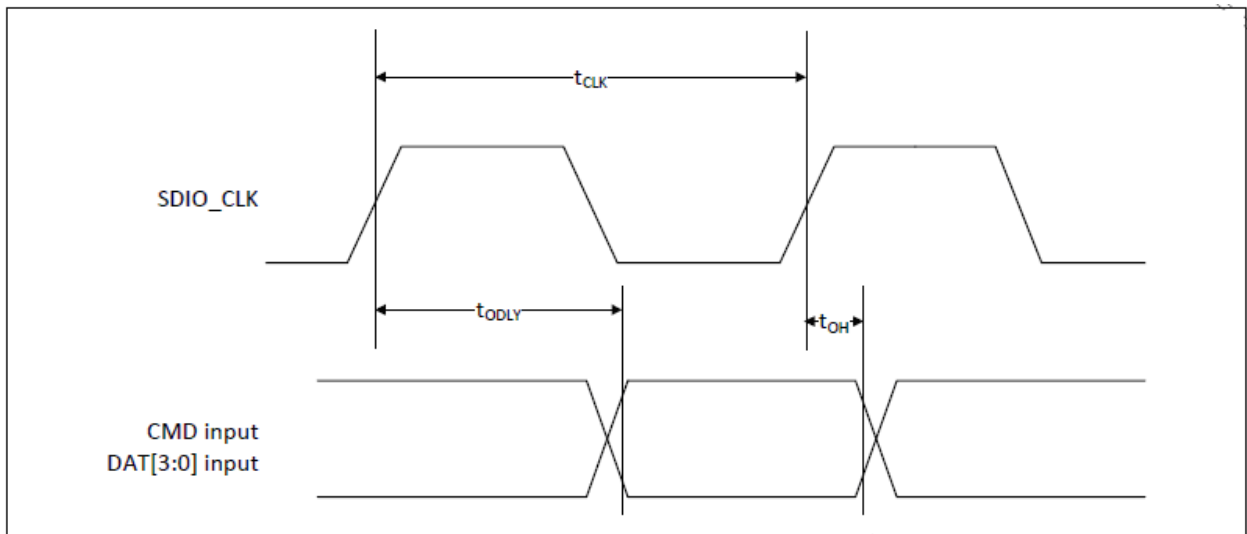
Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz, $C_{CARD} = 10$ pF
Clock duty	–	30	70	%	–

SDIO Bus Input timing (SDR Modes)



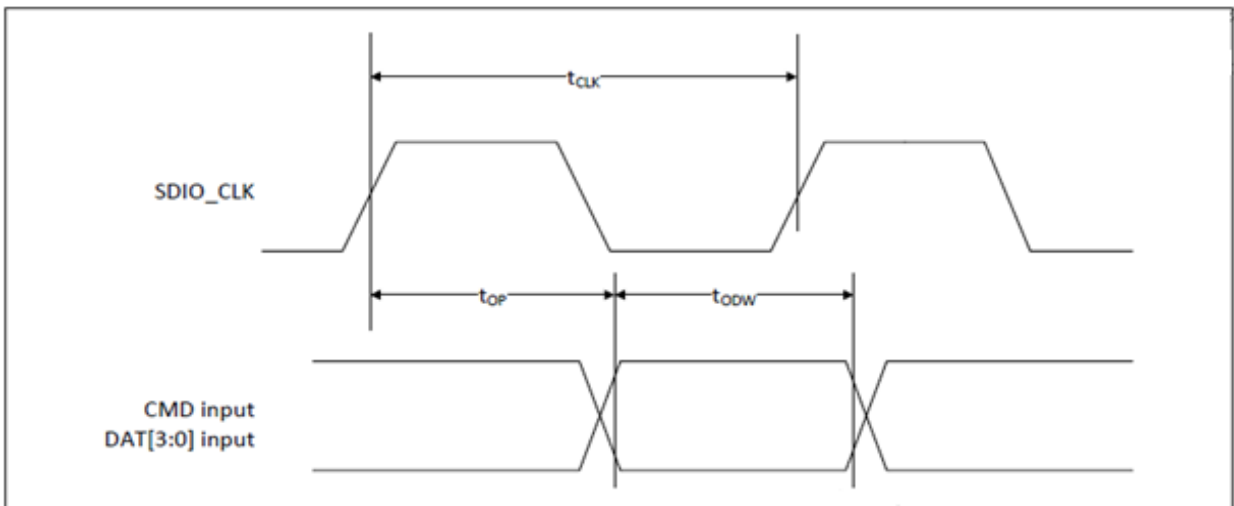
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	–	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

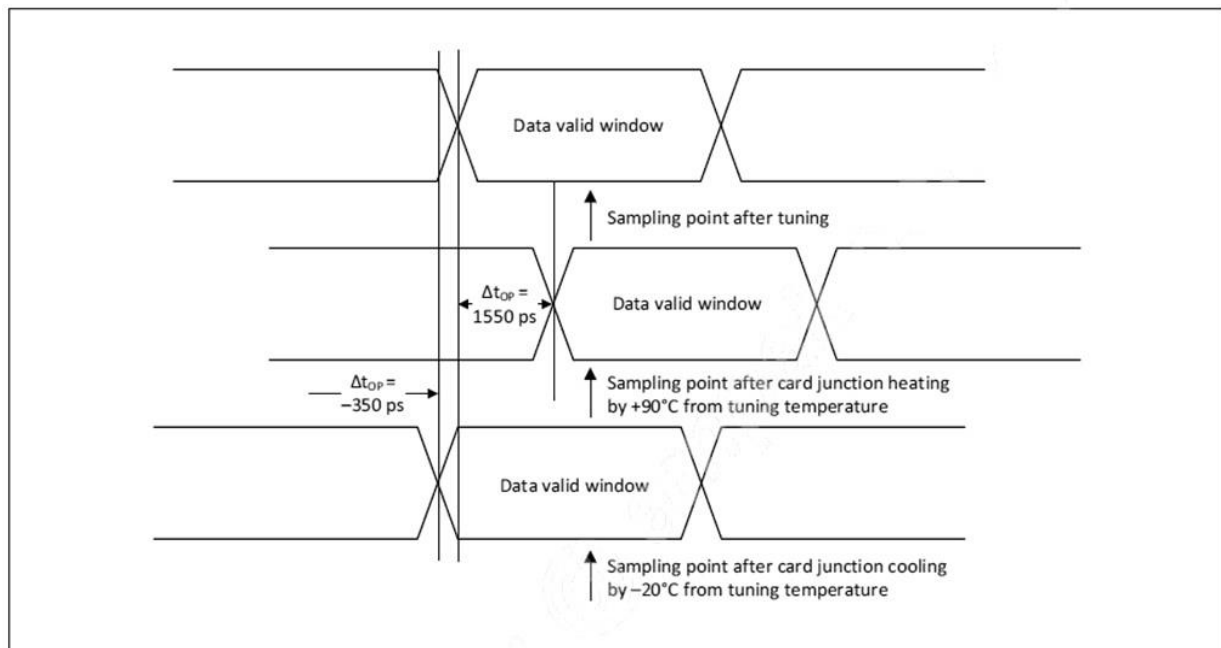
Card output timing (SDR Modes 100MHz to 208MHz)



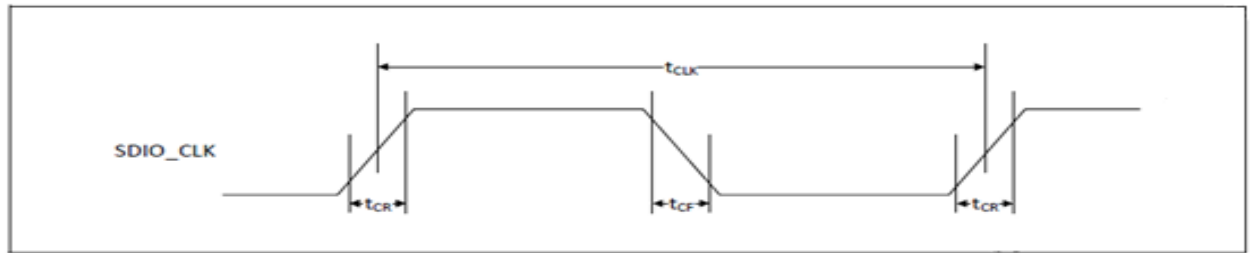
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	—	UI	$t_{ODW}=2.88$ ns @ 208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

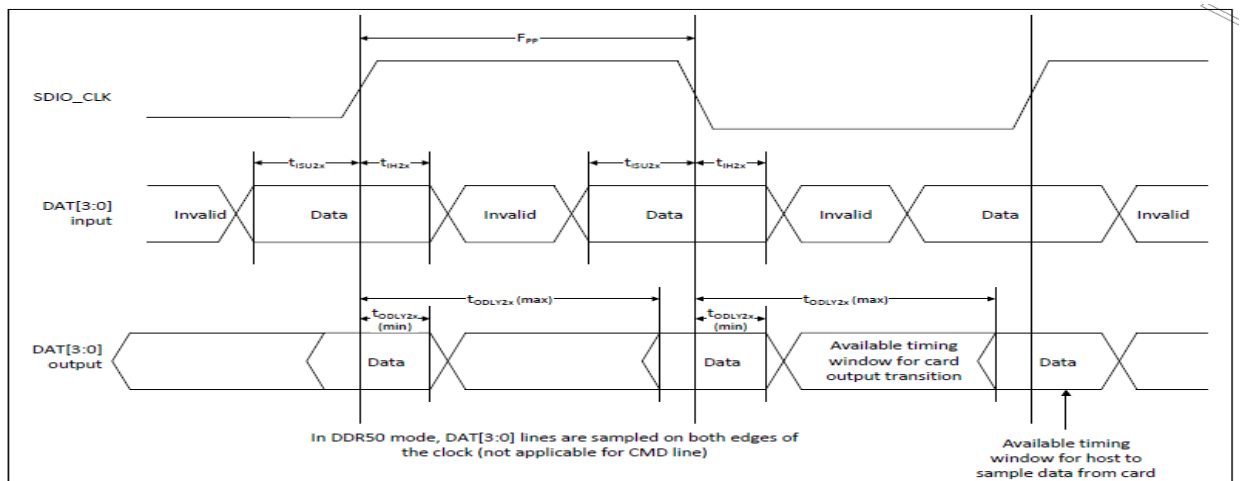


SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	20	—	ns	DDR50 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz, $C_{CARD} = 10$ pF
Clock duty	—	45	55	%	—

Data Timing



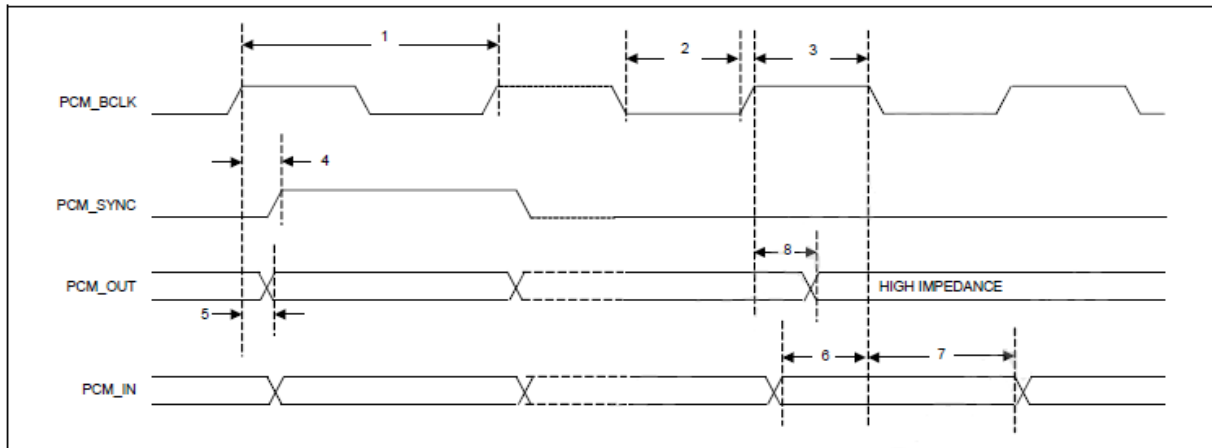
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	—	13.7	ns	$C_{CARD} < 30$ pF (1 Card)
Output hold time	t_{OH}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH2x}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	—	7.5	ns	$C_{CARD} < 25$ pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)

8.3 PCM Interface Description

The PCM Interface on the AP6275S can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP6275S generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP6275S. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

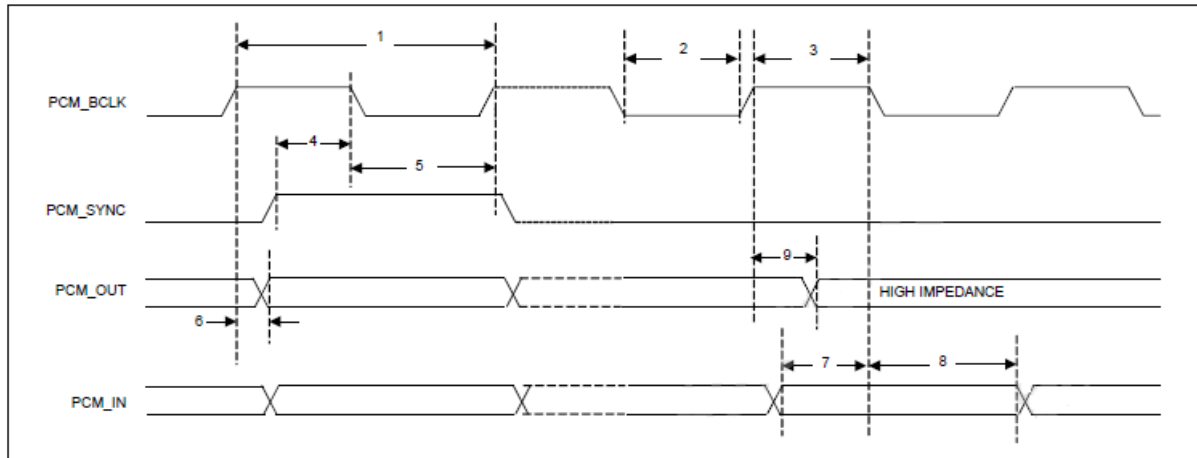


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

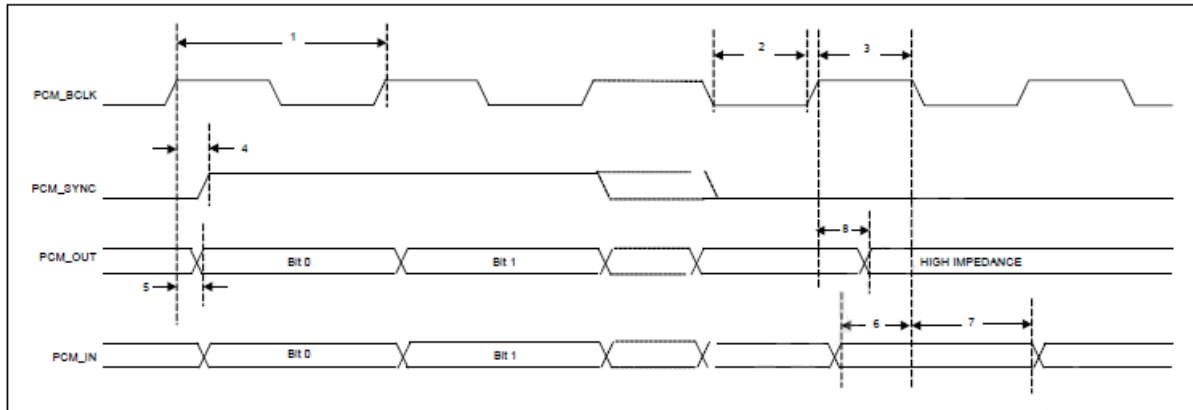


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

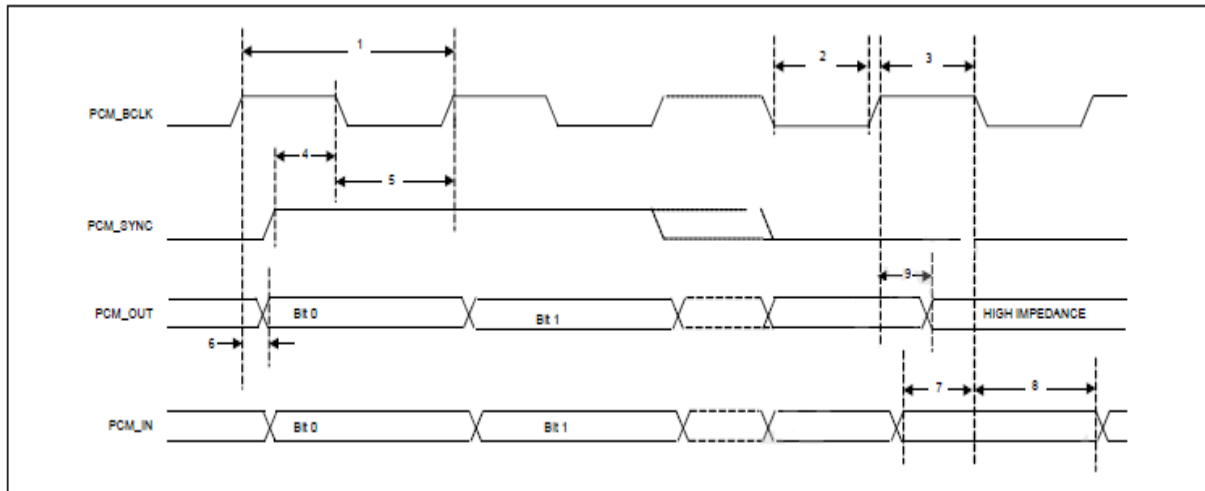


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

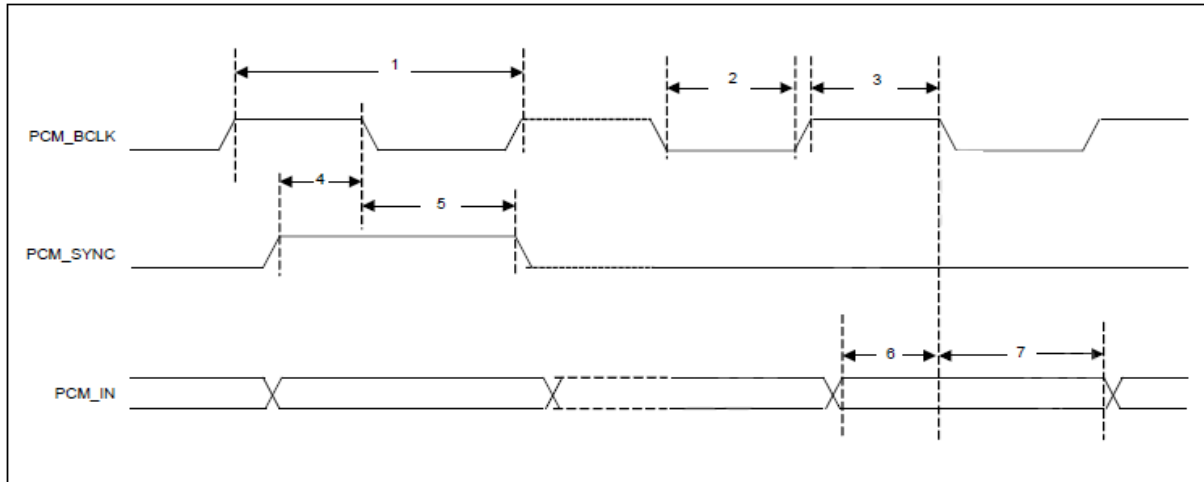


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

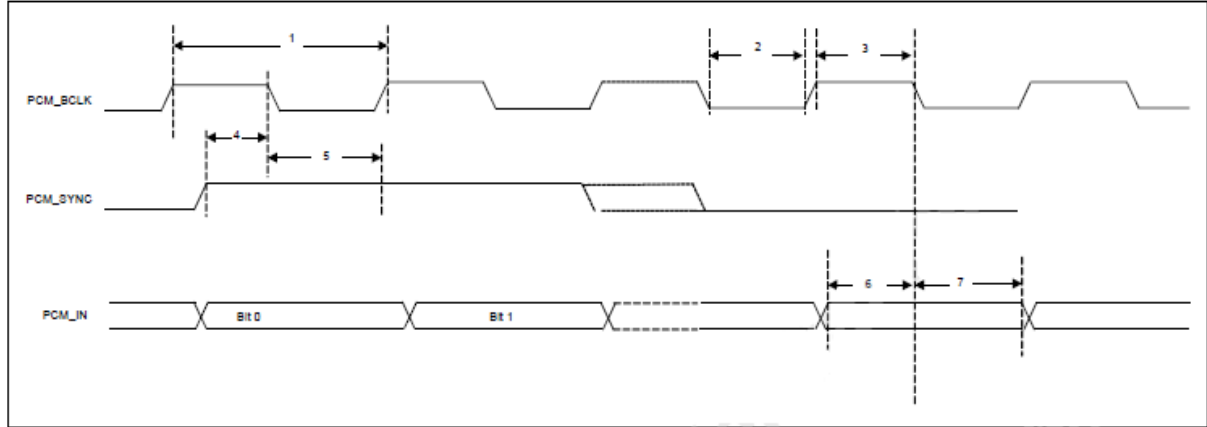


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

8.4 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

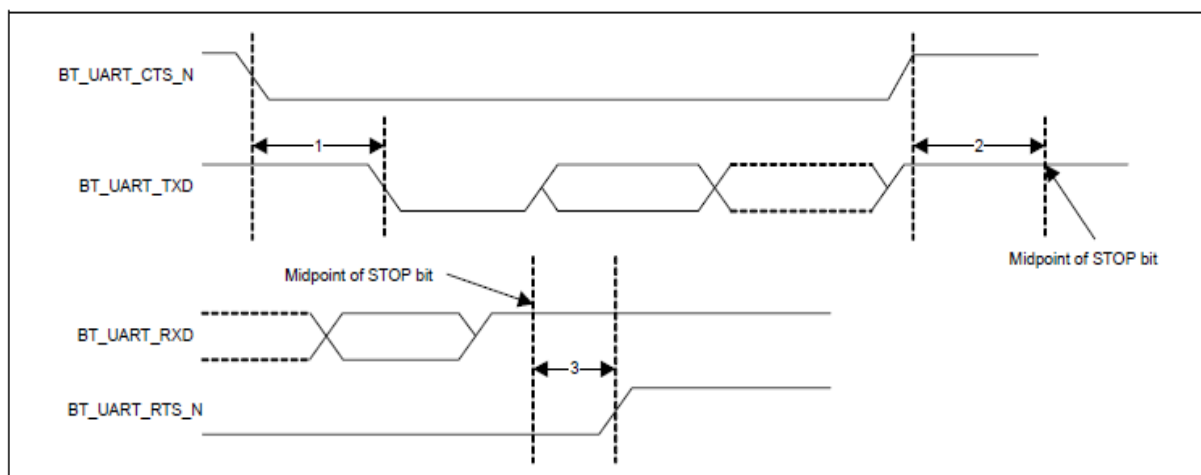
The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

Example of Common Baud Rates

<i>Desired Rate</i>	<i>Actual Rate</i>	<i>Error (%)</i>
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

UART Timing



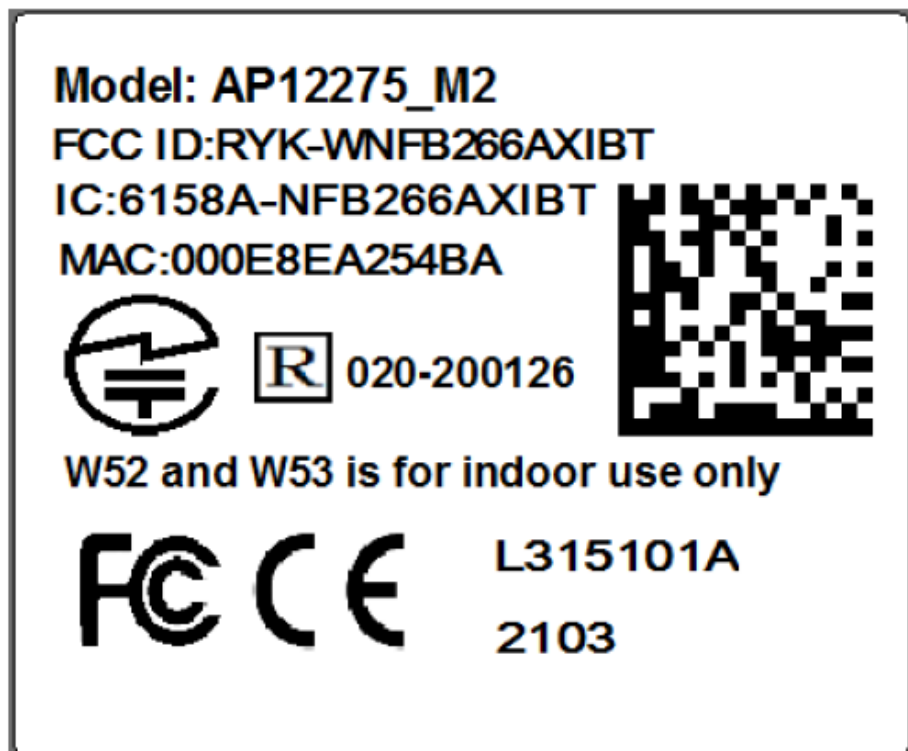
UART Timing Specifications

<i>Ref</i>	<i>Characteristics</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>	<i>Unit</i>
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

9. Package Information

9.1 Label

9.1.1 Product Label



9.1.2 Box Label

Label A

PO :	
AMK Device:	
PKG S/N :	
Model Name:	AP12275_M2 (R3HF)
P/N :	99P-W02-0560R
Quantity :	100
Date Code :	2021
Lot Code :	T314501D
	Made in Taiwan

Label Size: 70mmX50mm

[依各廠實際Label 使用]

(1)Barcode (BC) Symbology: Code128 Auto

(2)Human Readable: Arial

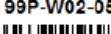
[字高依Label尺寸微調, 字體不可斷字,
條碼不可模糊,需可清晰讀取,辨識]



(Label A)

9.1.3 Carton Label

Label B

AMPAK Technology Inc.	
PO :	
AMK DEVICE:	
Model Name:	 AP12275_M2 (R3HF)
Part No :	 99P-V02-0560R
Quantity:	 400
Lot D/C :	 T3144009  2116
Manufacture:	 2021/04/28 Made in Taiwan

Label Size: 70mm X 100 mm
 [依各廠實際Label 使用]
 (1)Barcode (BC) Symbology: Code128 Auto
 (2)Human Readable: Arial
 [字高依Label尺寸微調, 字體不可斷字,
 條碼不可模糊,需可清晰讀取,辨識]



9.2 Tray box

1 tray/ box(100pcs/ tray box),

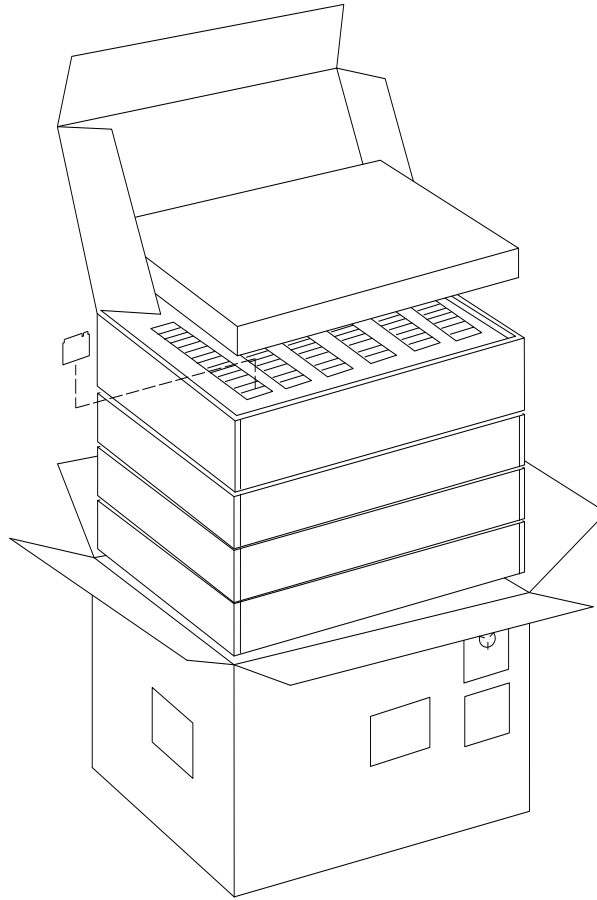


9.3 Carton

4 tray box/ Carton (400pcs/ carton)



9.4 Packing method



9.5 Ordering information

Item	Product Name	Description
1	AP12275_M2 (R3HF)	AP12275_M2 with RoHS compliant